Under the supervision of Dr. V. Prasad, Kyle Wilken and Aida Todri will use VHDL to design a RISC Processor for our senior project.

The main objective of our project is to design and implement a functional Reduced Instruction Set Computer (RISC) Processor using an FPGA. Our first step will be to research the RISC architecture and the feasibility of implementation using VHDL. We will then begin high-level design of the processor from a subsystem standpoint. Breaking the processor down into subsystems will allow both project members to work simultaneously on the design. Our processor will be developed and implemented on a Xilinx Development board using one of the XC4000e series of FPGA’s.