Matrix-Vector Multiplier Chip

General Description:

The Matrix-Vector Multiplier Chip will multiply a 3-bit x 3-bit matrix with a 3-bit vector to produce a 6-bit output. This chip utilizes a cellular array of CMOS elements, designed for easy expandability and testability. Each input pin accepts standard CMOS voltage levels. The outputs are also standard CMOS levels. For ease of testing, a sequence generator has also been added, which is accessible in test mode.

Specifications:

Supply Voltage ................................................................. 5V
Sink Current ................................................................. ?
Source Current ............................................................... ?
Power Dissipation ........................................................... ?
Fan Out ......................................................................... ?
Propagation Delay ......................................................... 10 cycles
Input Low Voltage ........................................................... 0-0.5V
Input High Voltage .......................................................... 4.5-5.0V
Output Low Voltage ......................................................... 0-0.5V
Output High Voltage ...................................................... 4.5-5.0V

| Clock Mode | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
|------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Vdd        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| Gnd        | NC| NC| NC| NC|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Y11        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| Y10        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| Y20        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| Y21        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| Y31        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| Y30        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| Y11        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| Y10        |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| Y20        | T1| T2| T3| T4| T5| TC1| TC2| TC3| TC4| TC5|

The clock pin is for a user-supplied clock input. Mode pin is 0 for normal operation and 1 for self-test operation. A1-3, B1-3, and C1-3 correspond to the inputs for the 1st, 2nd, and 3rd rows of the input matrix respectively. Pins X1-X3 correspond to the input vector. Y11 and Y10 are the bits of the 1st element of the output vector; likewise for Y21-Y20 and Y31-Y30. T1-T5 are active only in test mode. They are the outputs of each processor cell and pins TC1-TC5 are the carry bits from the processor cells.
Sample Operation

Mathematical representation of the chip’s function:

\[
\begin{pmatrix}
A1 & A2 & A3 \\
B1 & B2 & B3 \\
C1 & C2 & C3
\end{pmatrix}
\begin{pmatrix}
X1 \\
X2 \\
X3
\end{pmatrix}
= 
\begin{pmatrix}
Y11 & Y10 \\
Y21 & Y20 \\
Y31 & Y30
\end{pmatrix}
\]

A full truth table would be too large to include, but a couple examples are given:

Example 1:

\[
\begin{pmatrix}
1 & 1 & 0 \\
0 & 0 & 1 \\
1 & 1 & 1
\end{pmatrix}
\begin{pmatrix}
1 \\
0 \\
0
\end{pmatrix}
= 
\begin{pmatrix}
01 \\
00 \\
01
\end{pmatrix}
\]

Example 2:

\[
\begin{pmatrix}
1 & 1 & 1 \\
0 & 0 & 1 \\
1 & 0 & 1
\end{pmatrix}
\begin{pmatrix}
1 \\
1 \\
0
\end{pmatrix}
= 
\begin{pmatrix}
10 \\
00 \\
01
\end{pmatrix}
\]

The truth table for these two examples would look like this:

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>B1</th>
<th>B2</th>
<th>B3</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
<th>X1</th>
<th>X2</th>
<th>X3</th>
<th>Y11</th>
<th>Y10</th>
<th>Y21</th>
<th>Y20</th>
<th>Y31</th>
<th>Y30</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<td>0</td>
</tr>
</tbody>
</table>