Ultrasonic Signal Processing Platform for Nondestructive Evaluation

(usspnde)

Functional description and complete system block diagram

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Introduction

Ultrasonic nondestructive evaluation (NDE) has been widely used in quality assessment and failure analysis for critical structures or components in manufacturing, bridge structure, microelectronic packaging, and composite materials for aircraft structure. Different signal processing algorithms such as chirplet signal decomposition[1], Hilbert-huang transform [2], empirical mode decomposition [3], active noise cancellation [4], and Fractional Fourier transform [5] have been done for ultrasonic NDE application. Besides developing better signal processing algorithms, there is another important aspect of the challenge in ultrasonic industrial applications. That is, how to implement these algorithms efficiently on an embedded system.

The major challenges of ultrasonic system implementation are:

- High speed data acquisition and signal processing
  It is beneficial and practical to have real-time operation and detection with instantaneous results for ultrasonic NDE. The hardware and software components should be able to handle complex computations.
- Flexibility
  The system can be modified from time to time to take the advantages of evolving research results such as new processing algorithms. Configurable hardware makes it easy to implement future changes.

A conventional hardware design based on microcontrollers and digital signal processor falls short of meeting the demands of high speed, and adaptability requirements. This necessitates reconfigurable computing devices such as Field Programmable Gate Arrays (FPGA) to implement hardware and software co-design for the ultrasonic system.

This project aims to develop hardware and software for an ultrasonic signal processing system. The system can acquire ultrasonic data at 100M samples per second. An FPGA board is used to interface with an analog-to-digital converter (ADC) and a digital-to-analog converter (DAC).
A touch-screen LCD board is used to display ultrasonic signals. C language and VHDL are used for hardware/software co-design on the FPGA. An *EPOCH4* ultrasonic flaw detector is used as a reference to verify our design. The senior project design with reusable modules will be used as a general research and educational platform for ultrasonic signal processing at Bradley University.

Block Diagram

The high level block diagram is shown in Figure 1.

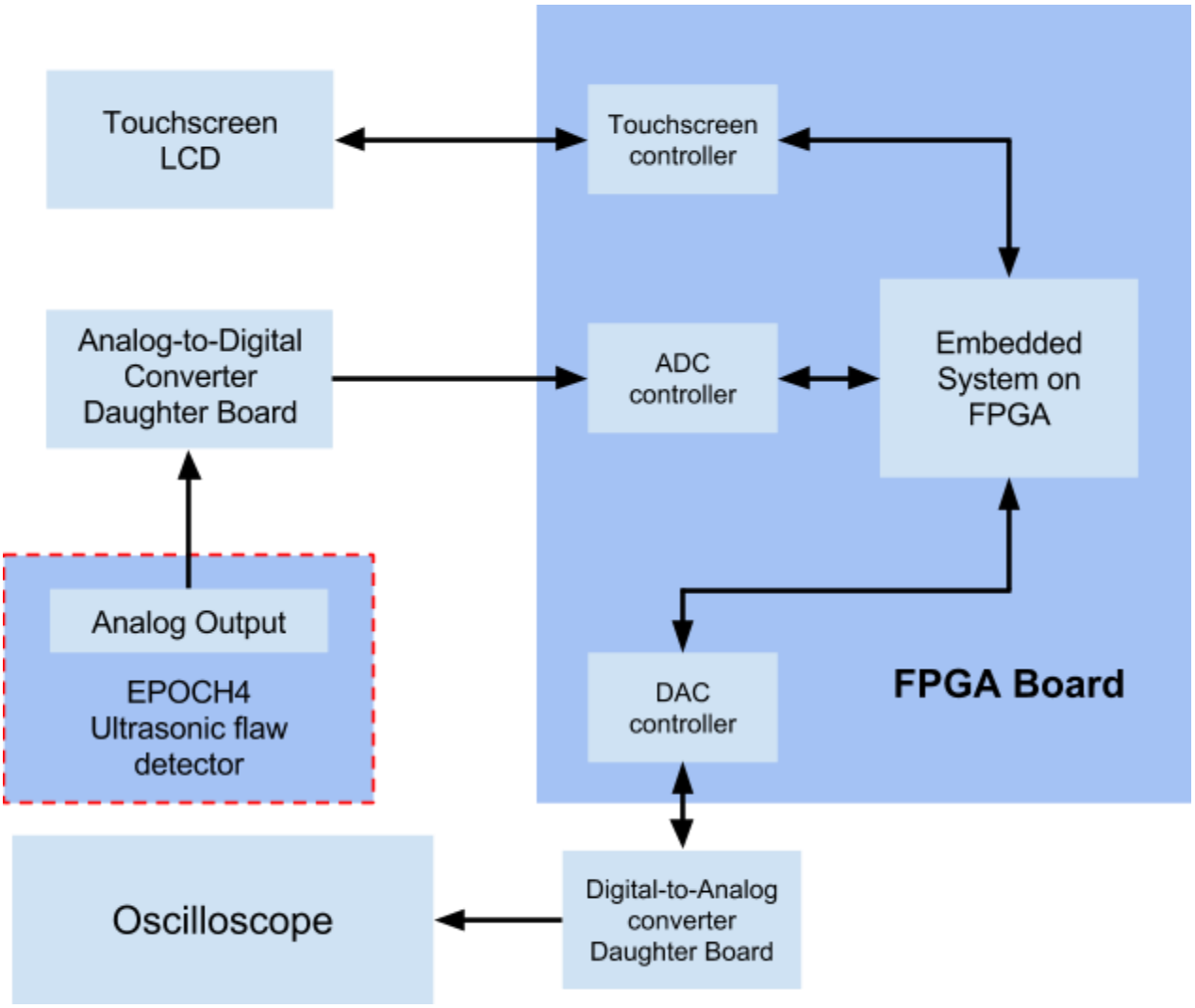

Figure 1- High Level Block Diagram

Functional Description

FPGA Board (Genesys Virtex-5 XC5VLX50T)

It mainly communicates with the peripherals such as the DAC board (MAX5874 EVKIT), the ADC board *(MAX1213N EVKIT)*, and the touchscreen display (Amulet STK-480272C). A standalone ultrasonic flaw detector, EPOCH 4, is used to provide an analog signal.

> ***Embedded system running on FPGA***
> A 32-bit RISC microprocessor, Microblaze is used in the embedded system. It runs at 100MHz frequency. C APIs are used to communicate with all peripherals. Except data acquisition and display, a signal processing algorithm can be added to the system.
>
> ***ADC controller (coded in VHDL)***
> It controls the ADC daughter board and receives a 12-bit data.
>
> ***DAC controller (coded in VHDL)***
> It controls the DAC daughter board and receives a 14-bit data.
>
> ***Touchscreen controller (coded in C)***
> It accepts touchscreen inputs and sends data outputs to the touch screen.

DAC board (MAX5874 EVKIT)

The board has the MAX5874 DAC device, which provides a sampling rate up to 200 MSPS. The resolution of DAC device is 14-bit. A oscilloscope is connected to the board for the purpose of display and verification.

ADC board (MAX1213N EVKIT)

The board has the MAX1213N ADC device. It provides up to 170 MSPS. The resolution is 12 bits.

Ultrasonic equipment (EPOCH4 ultrasonic flaw detector)

EPOCH4 is a standalone system for ultrasound flaw detection. In this project, it is used as a reference system to verify the project. Meanwhile, it provides an analog output for the project.

LCD touch screen (Amulet STK-480272C)

It is a 4.3” capacitive touch screen with the resolution of 480x272. A RS232 port is used to send inputs and outputs in the format of ASCII codes. It is used to display a variety of signals from the FPGA system.

Reference

[1] Y. Lu, R.Demirili, G.Cardoso, and J.Saniie, “A successive parameter estimation algorithm for chirplet signal decomposition”, *IEEE Transaction on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 53, no.11, pp. 2121-2131, November 2006.

[2] Y. Lu, E Oruklu, and J. Saniie, “Analysis of Hilbert-huang transform for ultrasonic nondestructive evaluation”, IEEE *International Ultrasonics Symposium 2008*, November 2-5 2008, Beijing, China.

[3] E. Oruklu, Y. Lu, and J. Saniie, “Hilbert transform pitfalls and solutions for ultrasonic NDE”, *IEEE International Ultrasonics Symposium 2009*, September 20-23 2009, Rome, Italy.

[4] D. Monroe, I. S. Ahn, and Y. Lu, “Adaptive filtering and target detection for ultrasonic backscattered signal”, *IEEE International Conference on Electro/Information Technology, May 20-22, 2010,* Normal, Illinois.

[5] Y. Lu, E. Oruklu, and J. Saniie, “Analysis of fractional Fourier transform for ultrasonic nondestructive applications”, *IEEE International Ultrasonics Symposium 2011*, October 18-21 2011, Orlando, Florida.