Ultrasonic Signal Processing Platform for Nondestructive Evaluation

(usspnde)

Functional Requirements List and
Performance Specifications

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Introduction

Ultrasonic nondestructive evaluation (NDE) has been widely used in quality assessment and failure analysis for critical structures or components in manufacturing, bridge structure, microelectronic packaging, and composite materials for aircraft structure. Different signal processing algorithms such as chirplet signal decomposition [1], Hilbert-Huang transform [2], empirical mode decomposition [3], active noise cancellation [4], and Fractional Fourier transform [5] have been done for ultrasonic NDE application. Besides developing better signal processing algorithms, there is another important aspect of the challenges in ultrasonic industrial applications. That is, how to implement these algorithms efficiently on an embedded system.

The major challenges of ultrasonic system implementation are:

- High speed data acquisition and signal processing

  It is beneficial and practical to have real-time operation and detection with instantaneous results for ultrasonic NDE. The hardware and software components should be able to handle complex computations.

- Flexibility

  The system can be modified from time to time to take the advantages of evolving research results such as new processing algorithms. A configurable hardware makes it future proof.

A conventional hardware design based on microcontrollers and digital signal processor falls short of meeting the demands of high speed, and adaptability requirements. This necessitates reconfigurable computing devices such as Field Programmable Gate Arrays (FPGA) to implement hardware and software co-design for the ultrasonic system.

This project aims to develop hardware and software for an ultrasonic signal processing system. The system can acquire ultrasonic data at 100M samples per second. An FPGA board is used to interface with an analog-to-digital converter (ADC) and a digital-to-analog converter (DAC). A touch-screen LCD board is used to display ultrasonic signals. C language and VHDL are used for hardware/software co-design on the FPGA. An EPOCH4 ultrasonic flaw detector is used as a reference to verify the system to be developed. The senior project design with reusable modules will be used as a general research and educational platform for ultrasonic signal processing at Bradley University.

Block Diagram

The high level block diagram is shown in Figure 1.

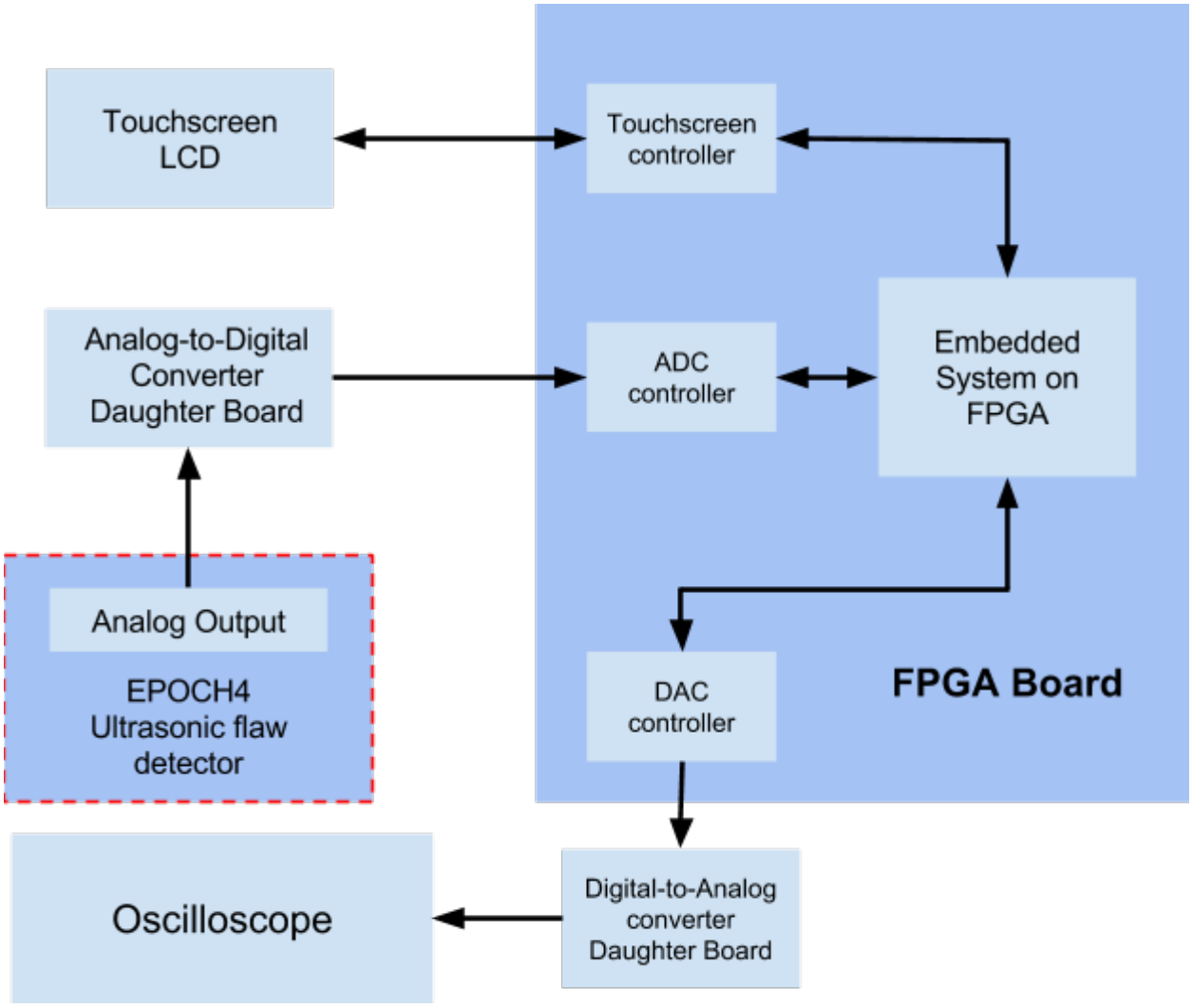

Figure 1. High Level Block Diagram of USSPNDE

System requirement and specifications

Hardware

FPGA Board (Genesys Virtex-5 XC5VLX50T)

- The main board in the system to be developed
- Interface with DAC and ADC peripherals through Very High Density Connection(VHDC)
- Interface with the touchscreen LCD board through UART
- Running under 100 MHz on-board system clock
- Others: 256 Mbyte DDR2 memory, 32 Mbyte flash memory and multiple USB2 ports.[8]

DAC board (MAX5874 EVKIT)

- MAX5874: A 14-bit, high-dynamic-performance DAC from Maxim Integrated, Inc.[6]
- Support update rates of 200 M samples per second.
- Operate under 3.3V and 1.8V supplies provided by the FPGA board and a MAX1536 voltage converter.
- Controlled by the 100 MHz clock signal from the FPGA board.
- Output a single-ended analog signal between 0 and 2Vpp

ADC board (MAX1213N EVKIT)

- MAX1213N: 12-bit low power ADC from Maxim Integrated, Inc.[7]
- Support a sampling rate up to 170 M samples per second.
- Operate under 3.3V and 1.8V supplies provided by the FPGA board and a MAX1536 voltage converter.
- Controlled by the 100 MHz clock signal from the FPGA board.
- Accept a single ended analog input signal between 0 and 2Vpp (EPOCH 4 ultrasonic flaw detector provides the analog signal source)
- Output 12 differential LVDS2.5 signals

LCD touch screen (Amulet STK-480272C)

- A LCD touch screen board used in past senior projects.
- Serial port communication protocol with 115200 BAUD rate
- Used as a peripheral of the embedded system running on the FPGA board.
- Other specifications: 480 X 272 resolution, refresh rate at 100 Hz.

EPOCH4 ultrasound flaw detector

- A standalone ultrasonic flaw detector
- Provide an analog reference to the senior project design
- The specifications of the analog output are to be investigated.

Software

Embedded system running on the Virtex-5 XC5VLX50T FPGA

- Use a 32-bit RISC Microblaze processor running at 100MHz.
- Development environment: Xilinx embedded development ki(EDK)/ software development kit(SDK)
- Save incoming data from ADC to the external DDR memory
- Accept the inputs from the GUI running on the touchscreen board.
- Languages to be used: C languages and VHDL
    - VHDL for the logic level hardware implementation of ADC and DAC controllers
    - C language for the drivers of ADC and DAC controllers, the interface of general purpose I/Os and UART, and signal processing algorithms running on the FPGA

ADC controller

- Implement the ADC controller in VHDL
- Provide C APIs for the ADC driver
- Accept 12 differential LVDS2.5 inputs from the ADC board
- Form a single-ended data vector for the signal processing algorithm.
- Include handshaking signals to control the data acquisition
- Operate at 100 MSPS

DAC controller

- Implement the DAC controller in VHDL
- Provide C APIs for the DAC driver
- Output a 14-bit data vector to the DAC board
- Operate at 100 MSPS

Touchscreen controller

- Implement the controller in C language
- Output ASCII data to the touchscreen board over RS232
    - [starting address in hex] [Upper nibble 1] [Lower nibble 1] [Upper nibble 2] [Lower nibble 2] … [Upper nibble N] [Lower nibble N] 0x00
    - Nibbles are in ASCII so to send hex value 0x80 send 0x38 as the upper nibble and 0x30 as the lower nibble
- Accept inputs from the touchscreen (ASCII format)
- Provide APIs for the embedded system running on the FPGA

References

[1] Y. Lu, R.Demirili, G.Cardoso, and J.Saniie, “A successive parameter estimation algorithm for chirplet signal decomposition”, IEEE Transaction on Ultrasonics, Ferroelectrics, andFrequency Control, vol. 53, no.11, pp. 2121-2131, November 2006.

[2] Y. Lu, E Oruklu, and J. Saniie, “Analysis of Hilbert-huang transform for ultrasonic nondestructive evaluation”, IEEE International Ultrasonics Symposium 2008, November 2-5 2008, Beijing, China.

[3] E. Oruklu, Y. Lu, and J. Saniie, “Hilbert transform pitfalls and solutions for ultrasonic NDE”,IEEE International Ultrasonics Symposium 2009, September 20-23 2009, Rome, Italy.

[4] D. Monroe, I. S. Ahn, and Y. Lu, “Adaptive filtering and target detection for ultrasonic backscattered signal”, IEEE International Conference on Electro/Information Technology,May 20-22, 2010, Normal, Illinois.

[5] Y. Lu, E. Oruklu, and J. Saniie, “Analysis of fractional Fourier transform for ultrasonic nondestructive applications”, IEEE International Ultrasonics Symposium 2011, October 18-21 2011, Orlando, Florida.

[6] MAXIM integrated, “MAX5873/MAX5874/MAX5875 Evaluation Kits” MAX5874 datasheet, [Revised June 2006].

[7] MAXIM integrated, “MAX1213N/MAX1214N Evaluation Kits” MAX1213N datasheet, [Revised July 2006].

[8] XILINX “ML505/ML506/ML507 Evaluation Platform: User Guide” XC5VLX110T datasheet, Nov. 2006 [Revised May 2011].