Reconfigurable Communication System Design

Functional Requirements List and Performance Specifications

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Introduction

Due to its reconfigurable ability and high throughput performance, Field Programmable Gate Array (FPGA) is widely used in embedded applications such as automotive, communication, industrial automation, motor control, medical imaging, to name a few. Quadrature Phase Shift Keying (QPSK) is one of the digital modulation standards used in third and fourth generation wireless communication systems. In this project, a reconfigurable communication system using QPSK modulation will be designed and implemented on an FPGA.

Some preliminary work has already been done at Bradley University. For example, a QPSK system has been implemented on a Virtex 4 FPGA board using MATLAB/Simulink and Xilinx system generator [1]. A random symbol generator and quadrature amplitude modulation (QAM) system have been worked in [2, 3]. The major drawback of Simulink-based tool is that the logic resource usage highly depends on the software automation and, thus, the design may not be compatible with different versions of software. A common complaint of hardware description languages (HDL) such as VHDL and Verilog HDL is that prior knowledge and experience in digital system design and programming details is required. On the other hand, HDL can provide a better solution in terms of logic resource usage and design compatibility. The goal of this project is to implement a complete QPSK system on FPGA boards using VHDL. The project aims to provide a reusable and efficient design for add-on features which may be needed at later times

Functional description and high level block diagram

Development of the QPSK system could be divided into three stages.

Stage 1 - single FPGA board prototype

The high level system block diagram of stage 1 is shown in Figure 1. In this stage, a single FPGA board will be used to prototype the QPSK system including random symbol generator, interpolator, up converter, down converter, decimator and digital-to-analog converter (DAC). Signals are routed internally from the transmitter to the receiver. A DAC is used to display data.

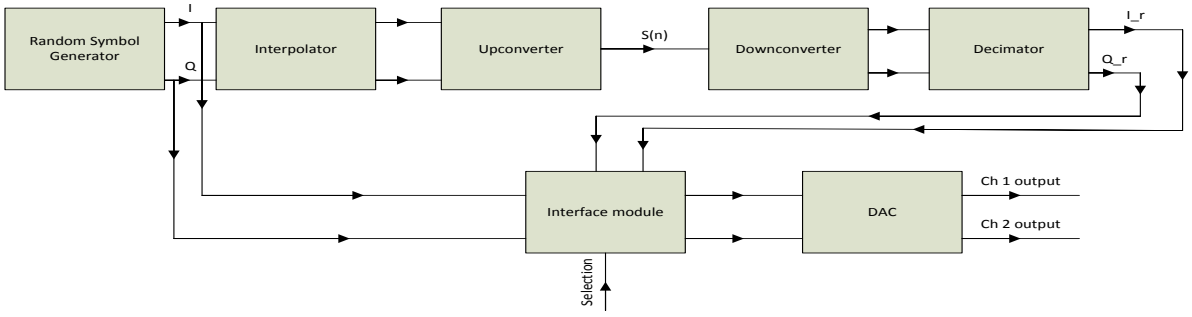

Figure 1. Stage 1 high level system block diagram

I = transmitter side in-phase
Q = transmitter side quadrature phase
I_r = receiver side in-phase
Q_r = receiver side quadrature phase

S(n) = internal signal from transmitter to receiver

Stage 2 - channel imperfection and carrier recover

The high level system block diagram of stage 2 is shown in Figure 2. In this stage, the transmitter and the receiver of QPSK system will be implemented on different FPGA boards. Compared with the system in stage 1, analog-to-digital converter (ADC) and DAC modules will be included in this stage. Adverse effects caused by channel imperfection will be discussed. Carrier recovery circuit and phase locked loop will be implemented in the receiver.

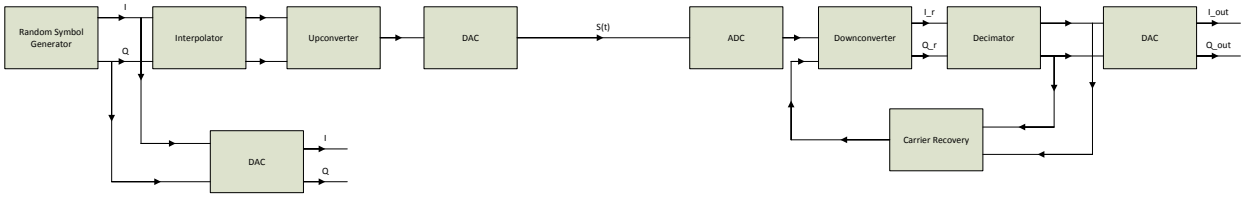

Figure 2. Stage 2 high level system block diagram

Stage 3 - system integration and evaluation

System integration and evaluation will be the focus of stage 3. High speed ADC and DAC modules will be used to connect the transmitter and receiver for assessing the overall system operations. Bit error rate (BER) of the system will be used as a metric to evaluate the overall system performance. Logic resource usage and module reusability will be monitored and continuously adjusted for fine tuning of the system throughout the project.

Functional Requirements

Stage 1 Requirements

- The DAC shall display the following: I(t) vs. Q(t), I(r) vs. Q(t), Q(t) vs. Q(r), and I(t) vs. I(r) based upon user input.
- The design shall be small enough to be implemented on a single Spartan 3E FPGA.

Stage 2 Requirements

- The signal DAC shall operate at a minimum of 1.4 MHz
- The ADC shall operate at a minimum of 1 MHz
- The sampling frequency shall satisfy Nyquist sampling theorem

Stage 3 Requirements

- The DAC speed shall be determined when hardware is chosen.
- The ADC speed shall be determined when hardware is chosen.
- A goal for BER shall be established.

References

[1] Anton Rodriguez, and Michael Mensinger Jr., "*Software-defined Radio using Xilinx*", Senior Project Report, Department of Electrical and Computer Engineering, Bradley University, Peoria Illinois, May 2011.

[2] Anthony Gaught, "*Software-defined Radio Symbol Generator*", Junior Project Report, Department of Electrical and Computer Engineering, Bradley University, Peoria Illinois, May 2012.

[3] Anthony Gaught, Alexander Norton, and Christopher Brady., "*FPGA-based 16 QAM communication system*", EE 568 Report, Department of Electrical and Computer Engineering, Bradley University, Peoria Illinois, April 2012.

[4] Leon Couch, *"Digital and analog communication systems"*, 8th ed., Boston: Pearson, 2013.

[5] Charles Roth Jr., and Lizy John, "Digital systems design using VHDL", 2nd ed., United States: Thomson, 2008.

[6] *Spartan-3E Data Manual*, Xilinx, San Jose, CA,2009.