Student :   Anthony Gaught

Title :   Reconfigurable Communication System Design

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Description :

      Due to its reconfigurable ability and high throughput performance, Field Programmable Gate Array (FPGA) is widely used in embedded applications such as automotive, communication, industrial automation, motor control, medical imaging, etc. QPSK is one of digital modulation standards used in the third and fourth generation wireless communication systems. In this project, a QPSK communication system will be designed and implemented on an FPGA.

      Designing an embedded system using hardware description language (HDL) requires a long training in digital system design and programming using, for example, VHDL. On the other hand, HDL can provide a better solution in terms of logic resource usage and design compatibility. In this project, VHDL is chosen for the hardware realization of a QPSK system on FPGA. The project aims to provide a reusable and hardware efficient design for future add-on features.

      The proposed QPSK system includes both transmitter and receiver sides. Raised cosine filter will be designed for reduction of intersymbol interference and conservation of transmission bandwidth. Phase locked loop will be studied and implemented for carrier recovery. Additionally, the performance of QPSK system will be evaluated in terms of bit error rate in conjunction with speed, area and power consumption among possible FPGA implementation options.