Active Noise Cancellation System

Functional Requirements List and Performance Specifications

Jessica Arbona & Christopher Brady

Dr. Yufeng Lu

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Introduction

The goal of the project is to design and implement an active noise cancellation system using an adaptive filter. Experimental data such as ultrasonic signal for nondestructive evaluation and recorded speech data will be used to test the system.

High Level Block Diagram

A high-level block diagram of an interference cancelling adaptive filter is shown in Figure 1.

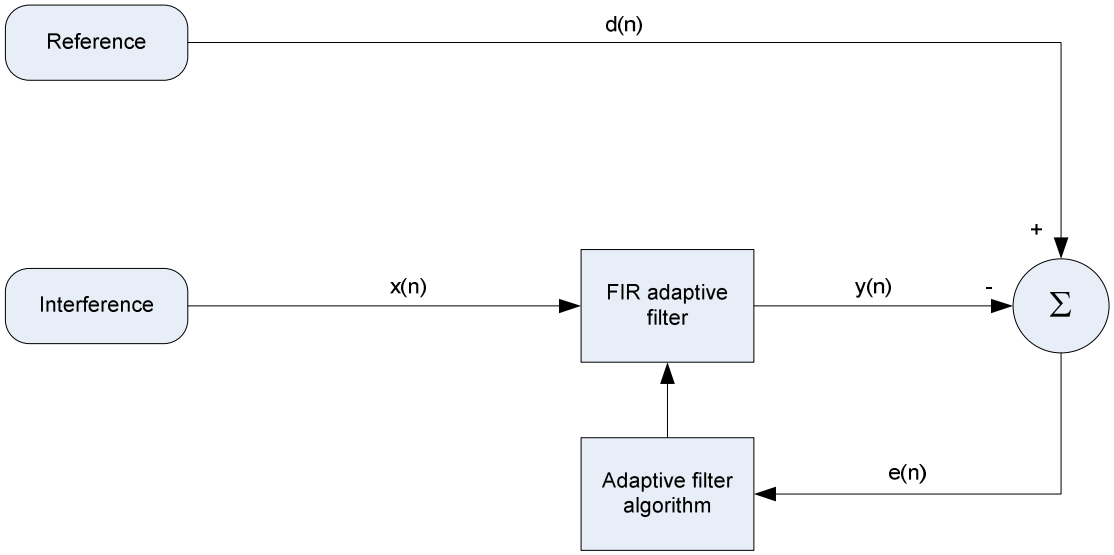

Figure 1 Block diagram of an active noise cancellation system

Functional Requirements List

Off-line ultrasound and speech data will be used to test the system. Ultrasonic data was acquired with a 5 MHz transducer and 100 MSPS sampling rate in an ultrasonic nondestructive data acquisition system. The adaptive filter will be designed using Xilinx system generator, a FPGA design tool incorporated in MATLAB/Simulink environment. An XtremeDSP development kit from Nallatch will be used as a platform to implement the adaptive filter. The FPGA device used in the project is Virtex 4 XC4SX35-10FF668. Two 14-bit DAC onboard channels (*AD9772 DAC devices*) will be used to probe the input and output of adaptive filtering system.

For speech signal processing, a SignalWave DSP/FPGA board from Lyrtech will be used to test the adaptive filtering system. An onboard audio CODEC (sampling frequency varies from 8 KHz to 48 KHz) is used for outputting signals. Real-time workshop and Xilinx system generator in MATLAB/Simulink will be used to compile the design. TI DSP (*TMS320C6713*) and Xilinx Virtex II FPGA (*XC2V3000-FF 1152*) devices will be used.

Performance specifications

Least mean square (LMS) adaptive filter will be implemented first. MATLAB simulation will be conducted to tune a step size for a good performance. Various pre-defined step sizes will be chosen for data sets from different applications. Different structures for LMS FIR filter will be designed and compared in terms of maximum frequency (minimal delay) and usage of logic resources. Hardware implementation of on-line step size calculation will be implemented as a comparison. Recursive least square (RLS) adaptive filter will be simulated second. Hardware implementation, especially matrix inversion, will be discussed and researched.