Comprehensive Ultrasound Research Platform

Functional Requirements List and Performance Specifications

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Introduction

The goal of this project is to create a prototype ultrasound research platform that will test theoretical developments on methods that use coded pulses to excite ultrasound transducers. These theoretical developments can then be compared to the current methods to conclude that a clearer ultrasound image is obtained. This prototype will test arbitrary waveforms on a multi-pin device, to compare experimental results with theoretical predictions. The preliminary results obtained in this project, by using devices that are already available or at a reasonable cost, will be used to guide the development of a future system (outside of this project's scope) using higher end components.

System Block Diagram

The steps are as follows: create an arbitrary waveform that will be used to excite an ultrasonic transducer, receive the backscattered echoes, process, and display an image. The excitation waveform must be initially transformed to sigma-delta modulation form to synthesize a digital-to-analog converter. As shown in Figure 1 below, the sigma-delta waveform will be stored in a memory device that is connected to an FPGA. The FPGA will be used to excite the transducer with the arbitrary waveform. Analog circuitry will be required to amplify and filter the digital output from the FPGA pins. After exciting the transducer with a voltage waveform, a pressure wave will propagate through the medium being imaged. The echo received by the transducer will be processed by the analog front end and stored on an embedded device. Finally, the stored data will be sent to a PC, processed, and displayed.

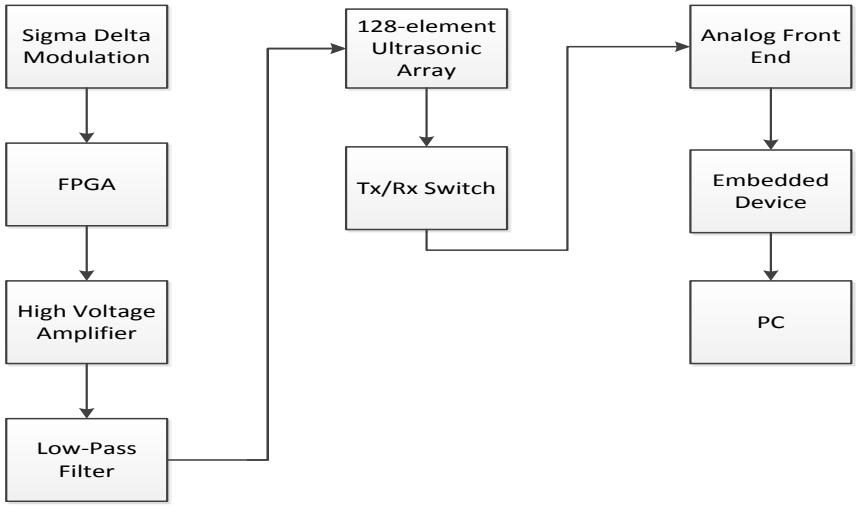

Figure 1: System Block Diagram

Functional Requirements

System Requirements

- The research platform will transmit and receive signals on up to eight channels on the transducer.
- Excitation waveforms shall be 3 μs or less in duration to maintain a time-bandwidth product of 40.
- Circuitry will be designed to achieve a signal to noise ratio greater than 50 dB.
- Resolution enhancement will create excitation signals capable of enhancing the bandwidth of the transducer to 12.45 MHz (150% of the center frequency of 8.3 MHz).

Transmitting FPGA

- The FPGA shall connect to the PC via Ethernet. The connection must be able to transmit 24 kbits of data to the FPGA in roughly 10 seconds (2.4 kbits/s) or less.
- The waveform data after being retrieved from the DDR2 shall be parallelized to prepare sending out on the FPGA pins. After parallelization, each pin shall change at a rate of 1 GHz.
- The waveform data to transmit must be stored in DDR2 memory when it is brought in from PC. Then it must be retrieved when the transmission occurs. The memory speed to support the 8 pin requirement is 62.5 MHz.
- The FPGA shall store independent sigma-delta encoded excitation waveforms of a maximum of 3072 samples for each of the eight channels.
- Each channel shall have a configurable delay of up to 5 μs relative to the other channels prior to transmission.
- The transmitting FPGA shall output a signal to the receiving FPGA when all excitations have been transmitted to start data collection.

Signal Conditioning

- Waveforms from the transmitting FPGA shall be amplified from ±1V (or 0 to 3.3V) to ±10V with a high speed op-amp. Slew rate for this op-amp shall be adequate to avoid distortion of the waveform.
- A second stage amplifier shall amplify the signals to ±100V to increase energy transmitted by the probe.
- A low pass filter shall decode the sigma-delta encoded waveforms into a chirp signal. The chirp shall match the desired waveform to within 10% mean squared error.

Receiving FPGA

- To simulate a pulse repetition frequency of 1 KHz, each channel will be recorded for 997 μs after all excitation waveforms have been transmitted for a maximum depth of 76 cm.
- Received signals shall be recorded using an A/D converter at a rate of 65 MHz and a resolution of 14 bits.

- The recorded data will be stored in DDR2 memory. The DDR2 memory speed shall be at least 65 MHz.
- Total data for 8 channels will be approximately 8 Megabytes.
- Data shall be transmitted to the PC in less than 10 seconds after full data collection using Ethernet (bit rate greater than 5.8 Mbit/s).

Data Processing

- All data processing shall be performed in less than 2 minutes.
- The image created will display an image for depths between 0.25 cm and 30 cm.