Real Time Video Capture and Image Processing System using FPGA

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Outline

☐ Introduction
☐ Goal
☐ Project Description
☐ Timeline
☐ Current Status
☐ Conclusion
Introduction

- Embedded System
  - Single function
  - Tightly constrained
  - Real-time
  - Hardware and software coexistence

- Current Technology
  - Microcontroller-based systems
  - DSP processor-based systems
  - ASIC technology
  - FPGA technology
Goal

☐ Design a real-time video capture and image processing system using FPGAs
Project Description

- Two Stages
  - Video capture and display
  - Video capture and image processing

- Hardware:
  - Xilinx Virtex II Pro FPGA board
  - Video decoder daughter board (VDEC1)
  - WT-300E camera (image size: 512 X 492)
Xilinx Virtex II Pro FPGA board
Video decoder daughter board (VDEC1)

- Component, composite, and S-video inputs
- I2C® compatible control bus
- High-speed Hirose FX2 data connector
- Supports NTSC, PAL, and SECAM inputs
- 8-bit or 16-bit YCrCb 4:2:2 outputs plus HS, VS and Field signals
- Programmable controls include peak white, brightness, saturation and contrast
Figure 1. System block diagram
Functional Specifications

- Able to capture an image and display on the monitor in real time.
- Contain the compatibility to configure the video decoder daughter board
- Color space change of video data
- Display the video data on a monitor by using Video Graphic Array (VGA) cable
- The image processing algorithms to process the video input data
- The video timing subsystem design to synchronize the video data input and output
Some details of the project

1. Design an embedded system to configure and drive the VDEC1 video decoder board
2. Develop data buffer and color-space change functions on the embedded system
3. Develop an image output function to drive the video digital-to-analog device and display the image on a monitor through XSGA port
4. Simulate the system using EDK tools, C, and hardware description languages and implement it on the Xilinx Virtex II Pro FPGA
5. Develop image processing functions in VHDL
6. Implement the video capturing and image processing system on the FPGA board
### TimeLine

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Current Progress

- Working on the tutorials of EDK tools
  - Design a simple embedded system using EDK
  - Add an IP block to the simple embedded system
  - Add a custom IP to the embedded system
  - Writing basic software application for the system
EDK Tools

- The Xilinx software suite for designing complete embedded programmable systems
- Enables the integration of both hardware and software components of an embedded system
Embedded Development Tool Flow Overview

1. VHDL or Verilog
   - HDL Entry
   - Simulation/Synthesis
   - Implementation
   - Download Bitstream Into FPGA
   - Chipscope

2. VHDL or Verilog
   - Standard Embedded SW Development Flow
     - Code Entry
     - C/C++ Cross Compiler
     - Linker
     - Load Software Into FLASH
     - Debugger

3. VHDL or Verilog
   - Embedded Development Kit
     - Board Support Package
     - System Netlist
     - Data2MEM
     - Download Combined Image to FPGA
     - Compiled ELF
     - Compiled BIT

Xilinx Workshop
Conclusion

- In this project, a video capture system will be implemented on the Xilinx FPGA board using Xilinx EDK tools.
- It will digitize the video signal from a camera and display it on the monitor in a real-time mode.
- Through this project, a hardware/software co-design method using FPGA will be explored for video and image processing applications.
Bibliography


Questions?

Thank you!
Functional Description

XUP-V2Pro Development System

VDEC1 Board

- Analog Interlaced Video
- Composite S-Video Component (YPbPr)

Video DAC

- 24 Bit RGB Video Data
- 858x525 pixels @ 60Hz

I2C Master

- Select the video source

XSGA Video Port

- De-interlace by line doubling

Monitor

- Select the video source

Video Decoder

- Digital Video
- ITU-R BT.656 YCbCr Data Format

Video Timing Extraction

- Video Timing Generation Logic
- Hsync Vsync Blanking Pixel Clock

Create the missing Chroma data samples

Color Space Conversion

- 4:2:2 YCrCb to 4:4:4 Conversion
- YCrCb to RGB Conversion

Line Field Decoder

- 4:2:2 YCrCb

Line Buffer (BRAM)

- Select the active line buffer for READS @27MHz
- Select the active line buffer for WRITES @13.5MHz

I2C Master

- De-interlace by line doubling

Buffer Control Logic

- Select the active line buffer for READS @27MHz
- Select the active line buffer for WRITES @13.5MHz

Buffer Control Logic

- Buffer Control Logic

Multiplexer

- Multiplexer

Line Buffer (BRAM)

- Line Buffer (BRAM)

Callouts:

- Video TIMing Generation Logic
- Digital Video
- ITU-R BT.656 YCbCr Data Format
- Video DAC
- 24 Bit RGB Video Data
- 858x525 pixels @ 60Hz
- I2C Master
- De-interlace by line doubling
- Line Buffer (BRAM)
- 4:2:2 YCrCb to 4:4:4 Conversion
- YCrCb to RGB Conversion
- Video Timing Extraction
- Video DAC
- XSGA Video Port
- Monitor
- Analog Interlaced Video
- Composite S-Video Component (YPbPr)

- Select the video source

- Video Timing Extraction
- Video DAC
- XSGA Video Port
- Monitor

- Analog Interlaced Video
- Composite S-Video Component (YPbPr)

- Select the video source
Functional Description

- VDEC1 Board
  - Video Decoder
  - I2C Master Bus
Functional Description

- XUP-V2 Pro Development System
  - Line Field Decoder
  - 4:2:2 to 4:4:4 Conversions
  - YCrCb to RGB Conversion
  - Buffer Control Logic
  - Line Buffer (BRAM)
  - Video Timing Generation Logic
  - Video DAC (Digital to Analog Converter)