Real-time Video Capture and Image Processing System using FPGA

Functional Description and System Block Diagrams

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**Introduction:**

This project aims to design a real-time video capture and image processing system based on the FPGA using Xilinx Virtex II-Pro board and VDEC1 video decoder daughter board. The project can be divided into two stages.

1. In the first stage, the video signal will be captured from the camera using VDEC1 board, and then the digitized signal will be buffered and converted in the Xilinx Virtex II-Pro board and sent to the monitor through SVGA port to display the image in real-time.

2. Based on the design from the first stage, image processing techniques such as convolution and edge-detections will be applied to the digitized video signal before it is displayed on the monitor. The add-on image processing functions should not comprise the real-time requirement of the system.

**Hardware design:** Xilinx Virtex II-Pro board and VDEC1 Video decoder daughter board are used in the project. The embedded design will be implemented in the Virtex II Pro FPGA device. And the camera, WT-300E NTSC, will be used as the video input. (The camera is under test now; it depends on the test result. A new camera may be purchased for the project).

**Software design:** VHDL, Verilog HDL, and C languages will be used to implement the system. All the design from these softwares will be incorporated into Xilinx Embedded Development Kit (EDK) environment to generate executable files for the embedded system.

**Project Goals:**

The main purpose of the project is to display a video signal on a monitor through the process of Xilinx Virtex II-Pro board. Image processing functions will be added to the system once it can display the image on the monitor. To achieve the project goal, the project is divided into the following steps:

- Design an embedded system to configure/drive the VDEC1 video decoder board.
- Develop the data buffer and color-space change functions on the embedded system.
- Develop an image output function to drive the video analog-to-digital device and display the image on the monitor through XSGA port.
- Implement the system using EDK tools, C and hardware description languages on the Virtex II Pro board.
- Develop image processing functions in VHDL language for the embedded system.
- Implement the video capturing and image processing system on the FPGA board.
Inputs of the System: A video input from the WT-300E camera, which is in NTSC format.

Outputs of the System: Display the processed images on the monitor.

**High-Level Block Diagram:**

![High-Level Block Diagram](image)

Figure 1: High-Level Block Diagram

The high level block diagram is shown in Figure 1. A camera is pointed towards the object to obtain the input, which is passed to the VDEC1 Video decoder daughter board.
The daughter board is connected to the Xilinx Virtex II-Pro board for further process. The input is sent to display on the monitor at the end of the process. Figure 2 shows the functional block diagram of the system with more details.

**Functional Description:**

As shown in Figure 2, the video data is captured from the camera through the video decoder board (i.e., VDEC1 board). Then, it is fed into the XUP-V2Pro development
platform for further processing. After the line buffering and color space converting process, the data is sent to XSGA port to display on the monitor. Furthermore, the programs running on the XUP-V2Pro board configure the video decoder board for the analog-to-digital conversion. The configuration information can be monitored using HyperTerminal through RS-232 port. The description of the subsystems in the functional block diagram is shown as following:

**VDEC1 Board**

**Video Decoder:**
Video Decoder board is used to digitize the video signal from the WT-300E camera at 27 MHz. It is configured using an FPGA IP through the I²C bus. It converts from an NTSC analog video data in YPrPb format, to the digital 10-bit video data in ITU-R BT.656 format, where ITU-R BT.656 is the video standard that contains color and brightness information in YCrCb format. All video field and line timing information are embedded in ITU-R BT.656. The 10-bit ITU-R-BT.656 YCrCb video signal and a 27 MHz clock is passed to the XUP-V2Pro Development System.

**I²C Master Bus:**
I²C bus is used to detect the video source type output from the WT-300E analog camera and select the same mode for the video decoder. It selects input from three different types:
- Composite Video Input (will be used in the project).
- S-Video Input
- Component Video Input

**XUP-V2 Pro Board**

**Line Field Decoder:**
Line Field Decoder obtains the digital video data from the video decoder, extracts the video timing information from the input signal and decodes the input signal into 4:2:2 YCrCb format. It provides downstream designs that consist of all the timing information, when the data is decoded.

**4:2:2 to 4:4:4 Conversions:**
It converts the signal fed by line field decoder from the 4:2:2 YCrCb format into 4:4:4 YCrCb format. It creates the missing chroma data samples, which is explained briefly in the next section.

**YCrCb to RGB Conversion:**
It converts the signal from the YCrCb format into RGB format after the conversion of 4:2:2 to 4:4:4 formats. The conversion is known as color space conversion that is explained in the next section.
Buffer Control Logic:
Buffer Control Logic controls two line buffers that also known as Block RAM (BRAM). It selects the active line buffers for READ signal at 27 MHz and for WRITE signal at 13.5MHz.

Line Buffer (BRAM):
It switches the functions of reading and writing at the end of the Read or Write Mode. When one BRAM is in READ mode other one is in WRITE mode and they will swap the functions at the end of the mode.

Video Timing Generation Logic:
It is used to generate an appropriate Hsync, Vsync, and blanking pixel clock from the timing data obtained from the line field decoder.

Video DAC (Digital to Analog Converter):
It inputs 24 bit RGB video data and convert it into the analog processing video signal to display on the monitor using 858x525 pixels format at 60 Hz.

Subsystem Description:

YCrCb to RGB Conversion (YUV color space conversion):
The input obtained from the Video Decoder is in YCrCb format, which is a standard version of YUV color model used in NTSC and other types of analog camera. YUV signal is generated from the RGB source format. Basically, R, G and B are embedded into the Y signal that corresponds to the brightness or luminance. U and V stand for the color information. Since the human eye is more perceptive to the luminance rather than color, the maximum bandwidth is utilized to store luminance data (Y) than color data (U and V). Therefore, the color difference components are used to reduce the bandwidth by one-third of the data. It is achieved by dividing a luma (Y) component into two color difference components (i.e., chroma- Cb/U and Cr/V). That means the brightness information (Y) is stored twice as much as color information (Cr, Cb).
The format of the information looks like YCrYCbYCrYCb…
After the 4:2:2 to 4:4:4 conversions, it converts back again into color information or RGB format that is standard format for most displays.

4:2:2 to 4:4:4 Conversions:
The main purpose of the conversion is to create the missing Cr and Cb components. It is processed by duplicating Cr and Cb components from the input at the previous cycle because Cr and Cb are inserted at every 2 clock cycles because they contain half as much brightness information. The format of the output looks like YCrCbYCrCb….

Video Timing Generation Logic:
The Video Timing Generation Logic is used to generate an appropriate Hsync, Vsync signals and blanking pixel clock from the timing data obtained from the line field
decoder. The information transmitted in the pixels must be synchronized with the timing signals in order to view at the monitor. The active period of the process is the period of the time when video data is being transmitted. The remaining portion is the blanking period, in which the sync pulse and other timing information is generated. The back porch is used to decode the color information from a composite signal. The front porch is used to insert a brief period between the end of each transmitted line and the leading edge of the next line.

**Conclusion:**
In the project, a video capture system will be implemented on the Xilinx FPGA board using Xilinx EDK tools. It will digitize the video from a camera and display it on the monitor in a real-time mode. Furthermore, through this project, a hardware/software co-design method will be explored for video and image processing.

**References:**


