Real Time Video Capture and Image Processing System using FPGA

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Outline

- Introduction
- System development
  - Video capture
  - Image processing
- Results
- Application
- Conclusion
- Bibliography
Embedded system

Specific application

Microcontroller

DSP processor

Tightly constrained (area, cost, time and power, etc.)

Embedded system

Hardware and software coexistence

ASIC

FPGA
Equipment

- 30,816 logic cells
- 138 18–bit multipliers
- 2,448 kB of block RAM
- PowerPc405 embedded processor

Virtex II Pro FPGA board
Equipment

- Component, composite and S–video inputs
- I²C® compatible control bus
- High–speed Hirose FX2 data connector

Video decoder daughter board
Embedded development kit (EDK) flow

1. Standard FPGA HW Development Flow
   - VHDL or Verilog
   - HDL Entry
   - Simulation/Synthesis
   - Implementation
   - Download Bitstream Into FPGA
   - Chipscope

2. Standard Embedded SW Development Flow
   - C Code
   - Code Entry
   - C/C++ Cross Compiler
   - Linker
   - Load Software Into FLASH
   - Debugger

3. Embedded Development Kit
   - Embedded Development Kit
   - Board Support Package
   - System Netlist
   - Data2MEM
   - Download Combined Image to FPGA
   - Compiled ELF
   - Compiled BIT

RTOS, Board Support Package
Load Software Into FLASH
Debugger

Xilinx Workshop
Objectives

What does the project do?
Project goals

- Design a real-time video capture and image processing system using FPGA
- System development
  - Video capture and real-time display
  - Video capture and image processing
System development

Video capture
Video capture

Video Input
- Video Input
- Digilent Video decoder daughter board
- Hirose socket connector

XUP Virtex II Pro board
- XSGA Video Port
- RS-232
- Console

Video Output
- **Video input**
  - Analog camera
    - Resolution: 512x492 pixels
    - Video output format: composite

- **Video output**
  - PC Monitor
Virtex-II Pro FPGA

XUP Virtex-II Pro main board
XUP-V2Pro Development System

VDEC1 Board

- Analog Interlaced Video
- Composite S-Video Component (YPrPb)

Video Decoder

- Line Field Decoder
- ITU-R BT.656 YCrCb Data Format

Video Timing Extraction

- 4:2:2 YCrCb

Create the missing Chroma data samples

Color Space Conversion

- 4:4:4 YCrCb to RGB Conversion

- 4:4:4 RGB

YCrCb to RGB Conversion

Buffer Control Logic

- Select the active line buffer for READS @27MHz
- Select the active line buffer for WRITES @13.5MHz

Line Buffer (BRAM)

Line Buffer (BRAM)

Multiplexer

Video DAC

- 24 Bit RGB Video Data
- 858x525 pixels @ 60Hz

Monitor

I2C Master

Select the video source

Select the video source

De-Interface by Line doubling

XSGA Video Port

I2C Master

Digital Video

Video Timing Generation Logic

- Hsync Vsync Blanking Pixel Clock

Video DAC

- Monitor

Audio DAC

- Audio Interface

Audio DAC

- Analog Processive Video

Video Timing Extraction

- 4:2:2 YCrCb

Create the missing Chroma data samples

Color Space Conversion

- 4:4:4 YCrCb
Specifications

- Developed in VHDL using EDK tools
- C language is used to configure the video decoder
- Supports NTSC and PAL inputs
- Output format (NTSC) : 858x525 pixels @60 Hz refreshing rate
System development

Image processing
Image processing

Video Input
- Digilent Video decoder daughter board
  - Hirose socket connector
    - XUP Virtex II Pro board
    - Image processing
  - Composite signal

Video Output
- XSGA Video Port

Console
- RS-232
Image processing

1. Brightening
2. Sharpening
3. Blurring
4. Edge detection
   1. Sobel x filter
   2. Sobel y filter
   3. Sobel xy filter
Work done

- Designed an embedded system to configure and drive the video decoder
- Developed video capture functions such as data buffer and color space conversions
- Developed a function to drive video DAC and display the image on the monitor through XSGA port
- Implemented image processing algorithms
Results

XUP-V2Pro Video Decoder Expansion Board Video Pass Through Test
Detecting Video Decoder... Configuring Decoder... SUCCESS!
Decoder detected! Configuring for composite video - default.

Mode Selection Menu
---------------------------------------------
1 - Program Composite Video Input Mode.
2 - Program S - Video Input Mode.
3 - Program Component Video Input Mode.
4 - Edit Setting Mode
q - Quit
Results

Original image

Brightened image
Results

*Sharpened image*  
*Blurred image*
Results

Edge detected image
Applications

- Medical imaging
- Digital cinema
- Surveillance
- Machine intelligence
- High definition TV
Conclusion

Completed

- Implemented real-time video capture system
- Successfully applied edge detection and other image processing algorithms
- Displayed real-time video data on monitor

Future Work

- Saving video data in memory
- Advanced image processing algorithms could be studied on the system for different applications.
Bibliography


Questions?

Thank you!
Thank you

- Dr. Yufeng Lu
- Dr. In Soo Ahn