Ultra Wideband Amplifier
Senior Project Proposal

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Senior Project

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1. Introduction

1.1 Ultra Wideband Overview

Ultra Wideband (UWB) communication is used for large bandwidth, low power, data transmission over a short distance. It is fundamentally different from other techniques because it uses extremely narrow Radio Frequency (RF) pulses to communicate between transmitters and receivers. UWB wireless transmission standard was approved for unlicensed use in 2002 under the FCC Part 15 [10]. This allows us to transfer data at high rate over a short distance. As shown in Fig 1.1-1 compared to other IEEE standards, UWB can transfer much greater data as long as the distance is a couple meters or less.

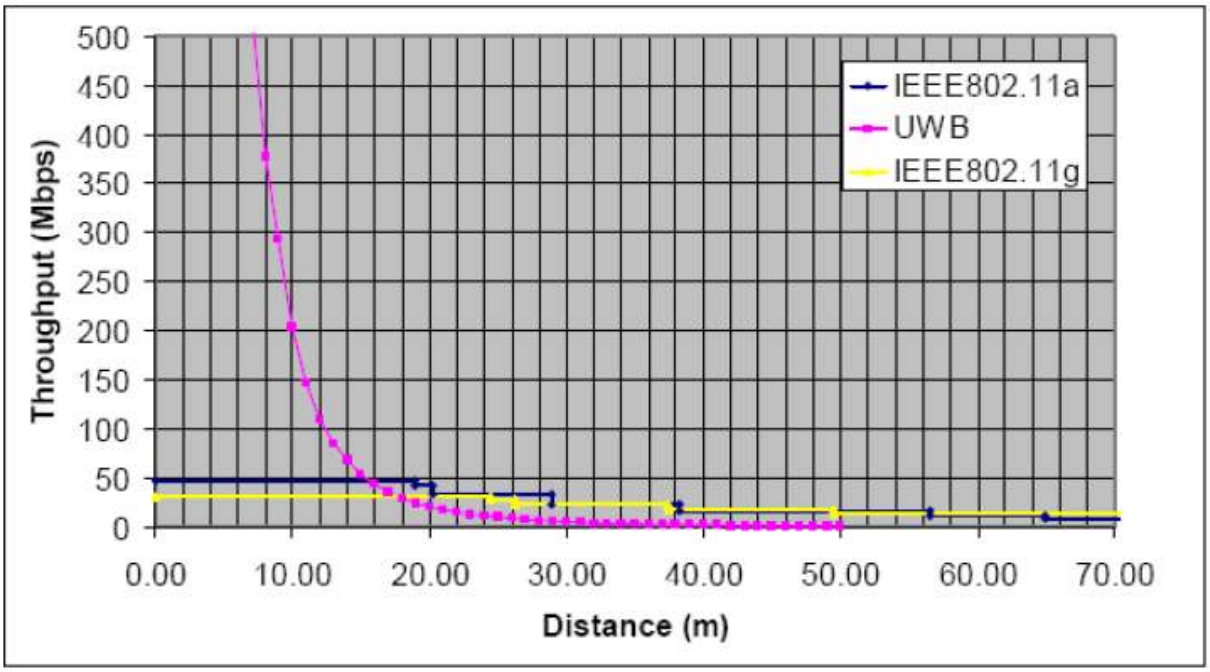


Fig 1.1-1: Transmission Rate vs. Distance

1.2 Project Summary

This project entails the usage of a low noise amplifier (LNA) with the topology of a distributed amplifier. The component fits on the receiver end of the UWB system, amplifying the incoming signal and rejecting all forms of external interferences.

2. Functional Description

2.1 System Block Diagram

A basic UWB system will have a signal pulse generator that generates a Gaussian pulse. The encoded signal is transmitted using the Gaussian pulses. The pulses are amplified and transmitted via antenna to the receiver. Once the receiving antenna receives the signal the low

noise amplifier will amplify the signal before it continues on into the receiver. Figure 2.1-1 shows the system block diagram. The LNA is the subsystem that we will design. The input to the LNA is the signal received from the antenna. The antenna receives the signal from the transmitting antenna.

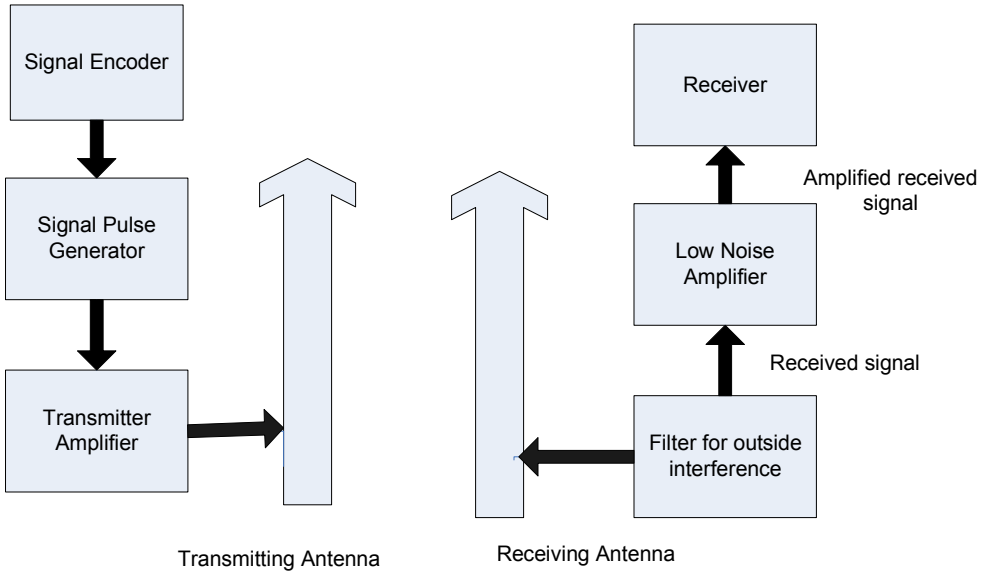


Figure 2.1-1: System Block Diagram of UWB System

2.2 Functional Requirements

The LNA will be a Gas FET transistor with a distributed amplifier topology. A prefabricated component will be used due to time limitations. The amplifier will amplify the signal coming from the receiving antenna without distortion and minimum power loss.

The amplifier must not interfere with outside frequencies and has to be able to operate correctly with outside interference. Table 2.2-1 shows all of the current frequency standards in the United States that will interfere with the UWB amplifier. These interferences may cause the amplifier to saturate. Design considerations will have to be done to avoid this. The exact effect of each frequency standard on the amplifier will be taken into account individually as the design process continues.

Standard	Frequency Range	Reference
IEEE 802.11a	5 GHz	[8]
IEEE 802.11i	2.4GHz and 5GHz	[8]
IEEE 802.16WiMAX	2GHz – 11 GHz	[9]

Table 2.2-1: Frequency Standards that will interfere with UWB

The required frequency range of operation is the entire UWB spectrum, 3.1 to 10.6 GHz. The desired cutoff frequency is 10.6 GHz. Amplifiers only get seventy percent of the maximum frequency desired. To get the desired cutoff frequency, the minimum f_{max} needed must be roughly 15 GHz as shown in equation 1. A maximum frequency of 20 - 25 GHz will be used to compensate for component loss.

EQUATION 1: $$\frac{10.6\,GHz}{.7} = f\,\max$$

2.3 Performance Specifications

A summary and comparison of various distributed amplifier specifications are shown in Table 2.3-1. These amplifiers are in the desired frequency ranges. Seeing these comparisons gives an idea of where to begin with the specifications for the amplifier. Table 2.3-1 lists several different designs done by others. Seeing the different topologies and their design results gave some insight on what design specifications to begin with. A median number was used to pick the specifications. These values are our tentative design goals. The specifications may change as the design process continues.

Desired Specifications:

Gain: 16 dB
Noise Figure: 2.5 dB
Power Dissipation: 60 mW

Reference	Gain (dB)	NF (dB)	BW (GHz)	PD (mW)	Topology	Technology
[1]	17.5	3.1	3.1-10.6	33.2	Distributed	0.18 µm CMOS
[2]	10	6.4	3.1-10.6	5.4	Distributed	0.35 µm SiGe BiCMOS
[3]	9	5.3	3.1-10.6	22	Distributed	0.18 µm CMOS
[4]	20	6.5	1.6-12.1	40	Low Power Distributed	0.35 µm SiGe BiCMOS
[5]	7.3	4.3-6.1	0-22	53	Distributed	0.18 µm CMOS
[6]	10.6	3.4-5.3	0-14	52	Distributed	0.18 µm CMOS
[7]	6	6	1-27	68.1	Distributed	0.18 µm CMOS

Table 2.3-1: Summary and Comparison of Distributed Amplifier Specifications

3. Regulations

3.1 FCC Regulations [11]

The minimum bandwidth must occupy more than 20% of the center frequency.
The minimum bandwidth must exceed 500 MHz.

3.2 Patents [11]

7139454 Ultra-wideband fully synthesized high-resolution receiver and method
7099422 Synchronization of ultra-wideband communications using a transmitted reference preamble
7061442 Ultra-wideband antenna
7020224 Ultra-wideband correlating receiver

3.3 Patent Applications [11]

20060165155 System and method for ultra-wideband (UWB) communication transceiver
20060062277 Ultra-wideband signal amplifier
20060045134 Ultra-wideband synchronization systems and methods

3.4 Standards [11]

ECMA 368 – High Rate Ultra Wideband PHY and MAC Standard
ECMA 369 – MAC-PHY Interface for ECMA-368

4. Equipment List

Network analyzer
Advance Microwave Lab Facilities
Transistor Package NE4210S01 – See Appendix A for data sheet
Board (To be determined)

5. Design

5.1 Lumped Element Calculations

The capacitors and inductors used in the lumped element model must be derived before simulation can begin. Using the equations found in Appendix F the capacitors and inductors used in the model were found. The steps to derive these values are also listed in Appendix F.

The final values for the capacitors and inductors are seen Below.

L = .795nH
L1 =.2385nH
L2 =.422nH
C1 =.0955pF
C =.318pF
C_d = .1494pF

No C_g is needed because the input capacitance is high enough.

5.2 Simulation of DC – IV Curves

The transistor was simulated using its nonlinear model represented in Appendix A. This model was provided in a library in a software package, Advanced Design System (ADS). The nonlinear model was built and simulated in this software package. See Fig B-2 in Appendix B for the

schematic of the circuit used to get the DC – IV curves. The simulation results are shown in Appendix D. Fig D-1 shows the Data sheet transistor DC – IV curves. This is compared to the simulation DC – IV curves shown in Fig D-2. They are similar until the drain to source current reaches 30mA. After this, the similarities disappear.

A bias point Q is found at the point where noise figure is lowest. The data sheets give this specification as Vds = 2 V and Ids = 10mA. The bias point chosen is -.6 drain to source voltage at 10mA for the drain to source current.

5.3 Scattering Parameter Simulations

The schematic in Appendix B shown in Fig B-2 was used to gather the S-parameters shown in Appendix C. These parameters measure just one transistor in the lumped element model. The capacitors and inductors designed in section 5.1 were used in the schematic. These parameters will be compared later to actual measured scattering parameters from the network analyzer after fabrication has taken place.

5.4 C_{in} and C_{out} Calculation

The schematic shown in Appendix C Fig C-2 was used to simulate and calculate the C_{in} and C_{out} values. Appendix E has the simulation results. The values for C_{in} was found to C_{in} = .333pF and C_{out}= .1686pF. These capacitors help to determine if padding capacitors are necessary. As seen in section 5.2 a drain padding capacitor was necessary but not a gate padding capacitor.

5.5 Design Steps Yet To Be Taken

The microstrip circuit still has yet to be designed. After the microstrip circuit is design simulations will be done to gather scattering parameters. The fabrication process is next. Once the amplifier is fabricated, parameters can be measured on the network analyzer. The measured values will be compared to those of the simulations. Ideally, these values should be very similar.

5.6 Design Tasks Time line

The time line can be found in Appendix G in Table G-1. The schedule of events is a rough idea of the tasks that need to be completed. The timeline will change as design work occurs since the exact time for fabrication and design work cannot accurately be calculated.

Appendix – A Transistor Data Sheet Schematics and S-Parameters

The transistor package NE3210S01 is seen in Fig 4-1. This is the schematic of the transistor pad layouts. Fig 4-2 shows the non linear model which is used in simulation software to measure scattering parameters, DC-IV curves and C_{in} and C_{out} values.

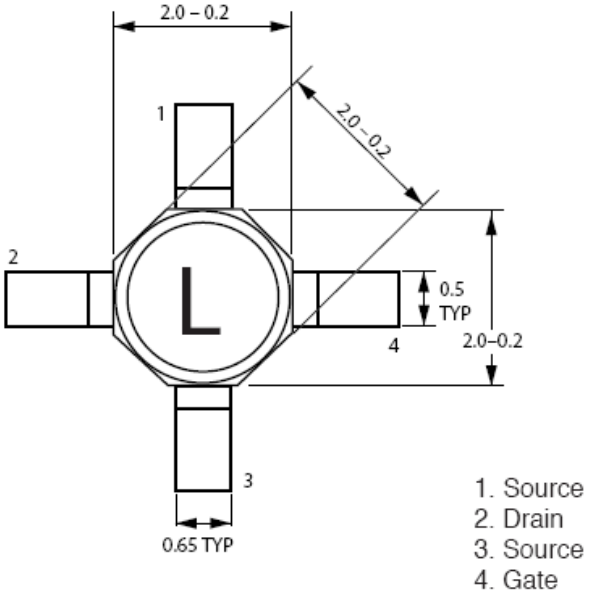


Fig 4-1: Transistor Package Outline

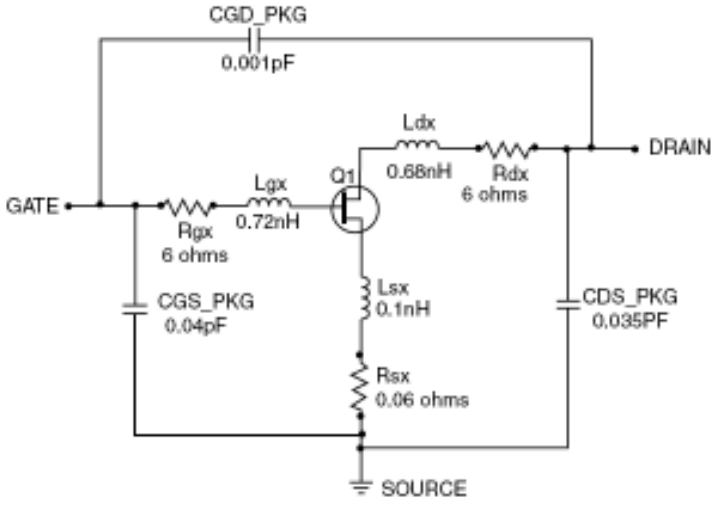


Fig 4-2: Nonlinear model of Packaged Transistor

Appendix B – Scattering Parameters

The scattering parameters from the Data sheet of NE3210S01 transistor are shown in Table 5.1 below.

VD=2 V, ID=5 mA	S11		S21		S12		S22	
Frequency (GHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
3	0.954	-32.09	3.388	142.45	0.041	65.57	0.698	-27.41
4	0.92	-43.04	3.381	129.89	0.053	54.85	0.67	-36.4
5	0.879	-53.83	3.387	117.91	0.062	45.72	0.638	-44.54
6	0.835	-64.32	3.428	106.08	0.07	38.3	0.604	-52.54
7	0.778	-77.53	3.525	92.97	0.081	29.68	0.533	-62.26
8	0.68	-92.29	3.539	78.21	0.086	17.34	0.469	-73.32
9	0.589	-109.87	3.527	63.32	0.091	7.85	0.398	-86.69
10	0.505	-127.92	3.432	49.9	0.089	0.93	0.335	-97.84
VD=2 V, ID=10 mA								
3	0.931	-35.15	4.754	138.61	0.037	65.91	0.614	-26.72
4	0.882	-46.86	4.663	125.12	0.047	56.77	0.583	-35.15
5	0.825	-58.15	4.565	112.41	0.055	48.65	0.549	-42.36
6	0.766	-68.97	4.529	100.03	0.061	42.3	0.515	-49.21
7	0.694	-82.82	4.537	86.54	0.07	34.76	0.463	-57.82
8	0.582	-97.9	4.418	78.98	0.074	24.44	0.38	-66.37
9	0.488	-116.4	4.301	57.78	0.079	16.93	0.314	-77.56
10	0.407	-135.11	4.109	45.24	0.08	12.32	0.261	-85.89
VD=2 V, ID=20mA								
3	0.908	-37.2	5.992	134.43	0.033	67.9	0.551	-24.92
4	0.845	-47.17	5.779	121.34	0.042	59.78	0.521	-32.4
5	0.777	-68.41	5.554	108.25	0.049	52.66	0.491	-38.3
6	0.709	-70.94	5.407	95.77	0.054	47.49	0.464	-40.02
7	0.63	-84.63	5.307	82.35	0.063	40.74	0.417	-51.35
8	0.513	-99.19	5.065	68.13	0.067	32.02	0.342	-57.35
9	0.42	-117.65	4.867	54.88	0.074	25.26	0.284	-66.38
10	0.342	-136.22	4.607	43.14	0.077	21.16	0.239	-72.34

Table 5-1: Scattering Parameters of Transistor Package from Schematic

Appendix C - Schematics

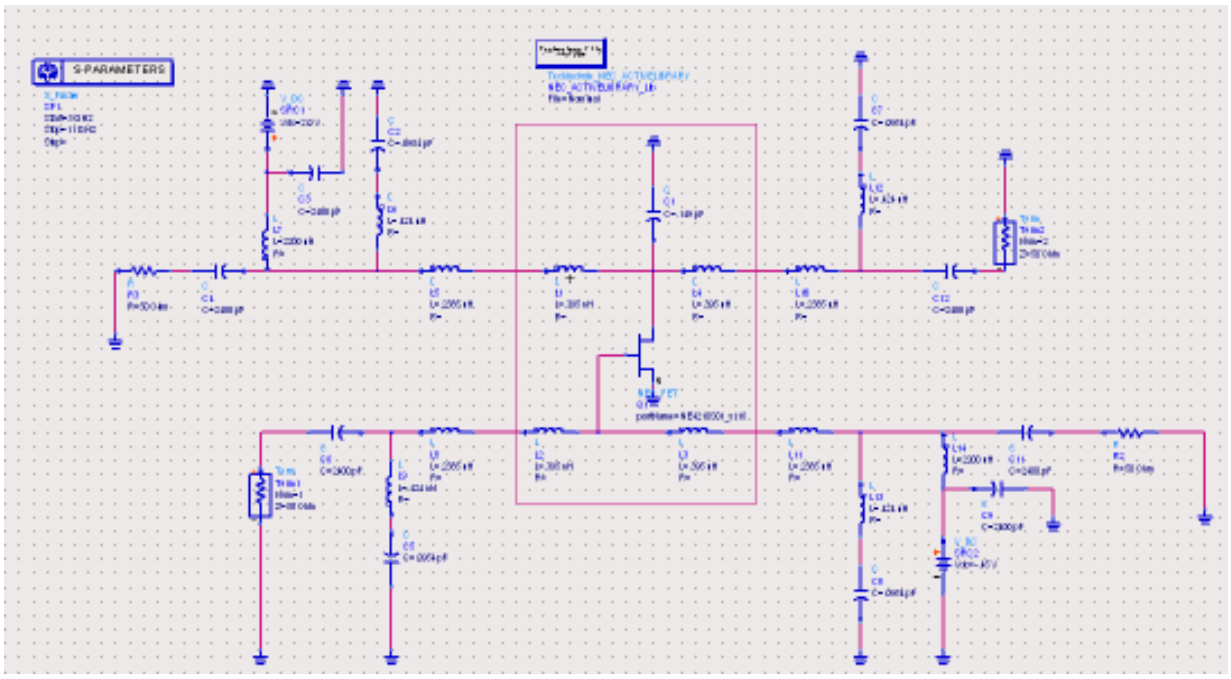


Fig 8-1: Distributed Amplifier with Single Transistor (Lumped Element)

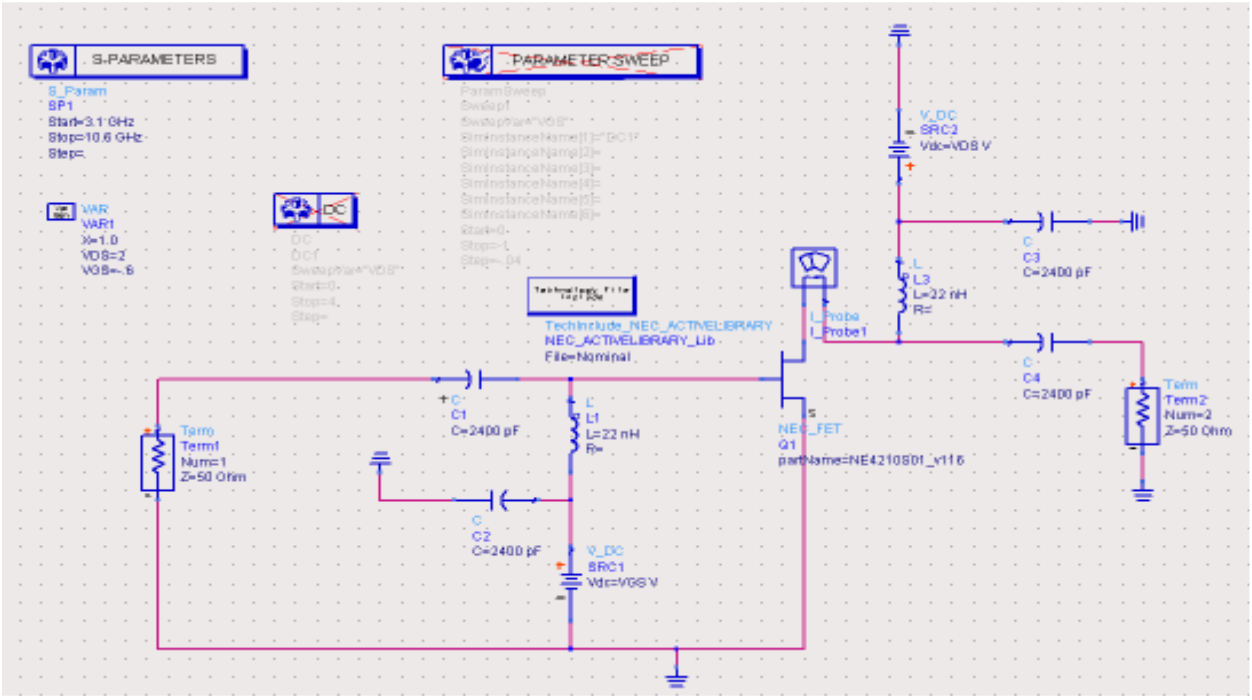
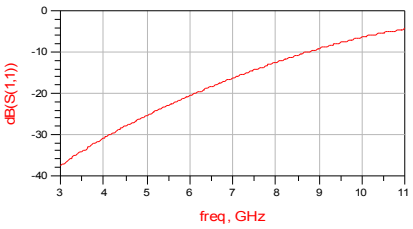


Fig 8-2: Schematic of Transistor Package

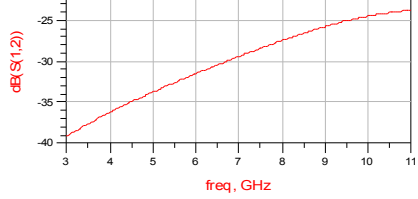
Appendix D - Scattering Parameters of Distributed Amplifier (Simulated)

freq	S(1,1)
3.000 GHz	0.013 / 175.646
3.040 GHz	0.014 / 175.796
3.080 GHz	0.014 / 175.934
3.121 GHz	0.015 / 176.059
3.161 GHz	0.015 / 176.172
3.201 GHz	0.016 / 176.272
3.241 GHz	0.016 / 176.361
3.281 GHz	0.017 / 176.438
3.322 GHz	0.017 / 176.505
3.362 GHz	0.018 / 176.560
3.402 GHz	0.018 / 176.605
3.442 GHz	0.019 / 176.640
3.482 GHz	0.020 / 176.664
3.523 GHz	0.020 / 176.679
3.563 GHz	0.021 / 176.684
3.603 GHz	0.021 / 176.680
3.643 GHz	0.022 / 176.667
3.683 GHz	0.023 / 176.645
3.724 GHz	0.023 / 176.614
3.764 GHz	0.024 / 176.575
3.804 GHz	0.025 / 176.527
3.844 GHz	0.026 / 176.471
3.884 GHz	0.026 / 176.406
3.925 GHz	0.027 / 176.334
3.965 GHz	0.028 / 176.254
4.005 GHz	0.029 / 176.166
4.045 GHz	0.029 / 176.071
4.085 GHz	0.030 / 175.969
4.126 GHz	0.031 / 175.859
4.166 GHz	0.032 / 175.742

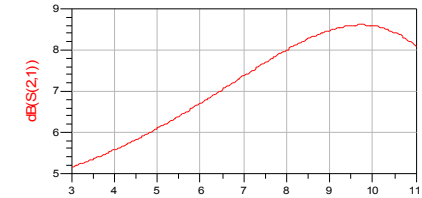
freq	S(2,2)
3.000 GHz	0.123 / 156.497
3.040 GHz	0.123 / 156.231
3.080 GHz	0.123 / 155.967
3.121 GHz	0.123 / 155.704
3.161 GHz	0.123 / 155.444
3.201 GHz	0.124 / 155.185
3.241 GHz	0.124 / 154.928
3.281 GHz	0.124 / 154.673
3.322 GHz	0.124 / 154.420
3.362 GHz	0.125 / 154.169
3.402 GHz	0.125 / 153.920
3.442 GHz	0.125 / 153.673
3.482 GHz	0.125 / 153.427
3.523 GHz	0.126 / 153.183
3.563 GHz	0.126 / 152.942
3.603 GHz	0.126 / 152.702
3.643 GHz	0.126 / 152.464
3.683 GHz	0.127 / 152.228
3.724 GHz	0.127 / 151.994
3.764 GHz	0.127 / 151.762
3.804 GHz	0.128 / 151.532
3.844 GHz	0.128 / 151.303
3.884 GHz	0.128 / 151.077
3.925 GHz	0.128 / 150.852
3.965 GHz	0.129 / 150.630
4.005 GHz	0.129 / 150.409
4.045 GHz	0.129 / 150.190
4.085 GHz	0.130 / 149.973
4.126 GHz	0.130 / 149.757
4.166 GHz	0.131 / 149.544

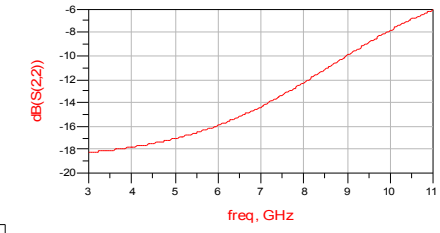


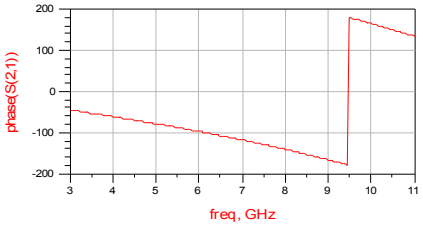
freq	S(1,2)
3.000 GHz	0.011 / -115.558
3.040 GHz	0.011 / -115.924
3.080 GHz	0.011 / -116.291
3.121 GHz	0.011 / -116.660
3.161 GHz	0.012 / -117.029
3.201 GHz	0.012 / -117.399
3.241 GHz	0.012 / -117.770
3.281 GHz	0.012 / -118.142
3.322 GHz	0.012 / -118.516
3.362 GHz	0.013 / -118.890
3.402 GHz	0.013 / -119.265
3.442 GHz	0.013 / -119.641
3.482 GHz	0.013 / -120.019
3.523 GHz	0.013 / -120.397
3.563 GHz	0.013 / -120.777
3.603 GHz	0.014 / -121.158
3.643 GHz	0.014 / -121.540
3.683 GHz	0.014 / -121.923
3.724 GHz	0.014 / -122.307
3.764 GHz	0.014 / -122.693
3.804 GHz	0.014 / -123.080
3.844 GHz	0.015 / -123.468
3.884 GHz	0.015 / -123.857
3.925 GHz	0.015 / -124.248
3.965 GHz	0.015 / -124.640
4.005 GHz	0.015 / -125.033
4.045 GHz	0.016 / -125.428
4.085 GHz	0.016 / -125.824
4.126 GHz	0.016 / -126.221
4.166 GHz	0.016 / -126.620



freq	S(2,1)
3.000 GHz	1.809 / -45.675
3.040 GHz	1.812 / -46.317
3.080 GHz	1.815 / -46.960
3.121 GHz	1.818 / -47.604
3.161 GHz	1.821 / -48.249
3.201 GHz	1.825 / -48.896
3.241 GHz	1.828 / -49.543
3.281 GHz	1.831 / -50.192
3.322 GHz	1.835 / -50.842
3.362 GHz	1.838 / -51.494
3.402 GHz	1.842 / -52.146
3.442 GHz	1.845 / -52.800
3.482 GHz	1.849 / -53.456
3.523 GHz	1.852 / -54.112
3.563 GHz	1.856 / -54.770
3.603 GHz	1.860 / -55.430
3.643 GHz	1.863 / -56.091
3.683 GHz	1.867 / -56.753
3.724 GHz	1.871 / -57.417
3.764 GHz	1.875 / -58.082
3.804 GHz	1.879 / -58.748
3.844 GHz	1.883 / -59.416
3.884 GHz	1.887 / -60.086
3.925 GHz	1.891 / -60.757
3.965 GHz	1.895 / -61.430
4.005 GHz	1.899 / -62.105
4.045 GHz	1.903 / -62.781
4.085 GHz	1.908 / -63.458
4.126 GHz	1.912 / -64.137
4.166 GHz	1.916 / -64.818







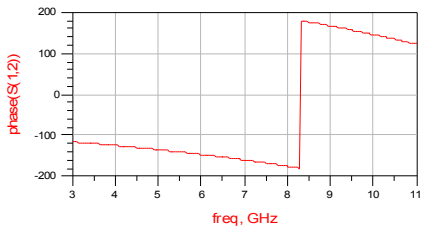


Fig 12-1: Scattering Parameters (Simulated)

Appendix D – DC-IV Characteristic Curves

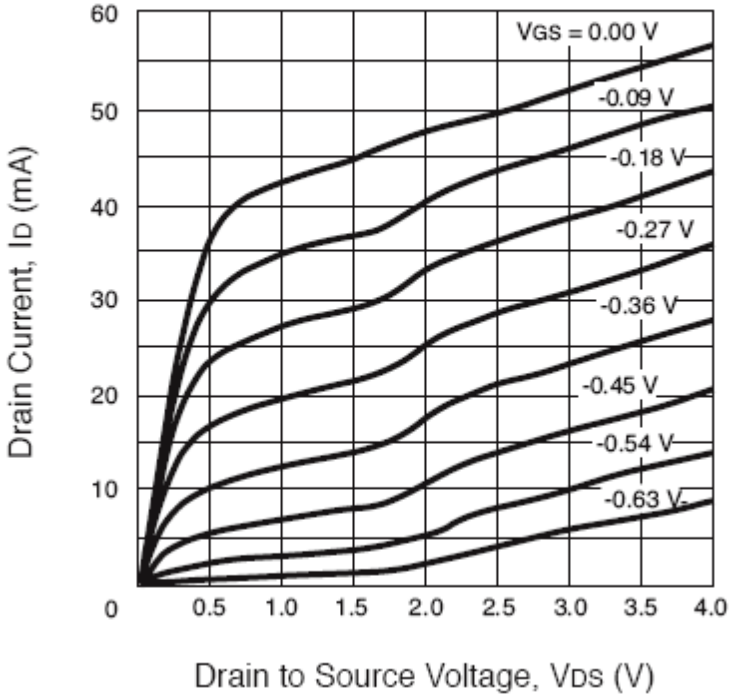


Fig 10-1 Drain Current VS Drain to Source Voltage Curves

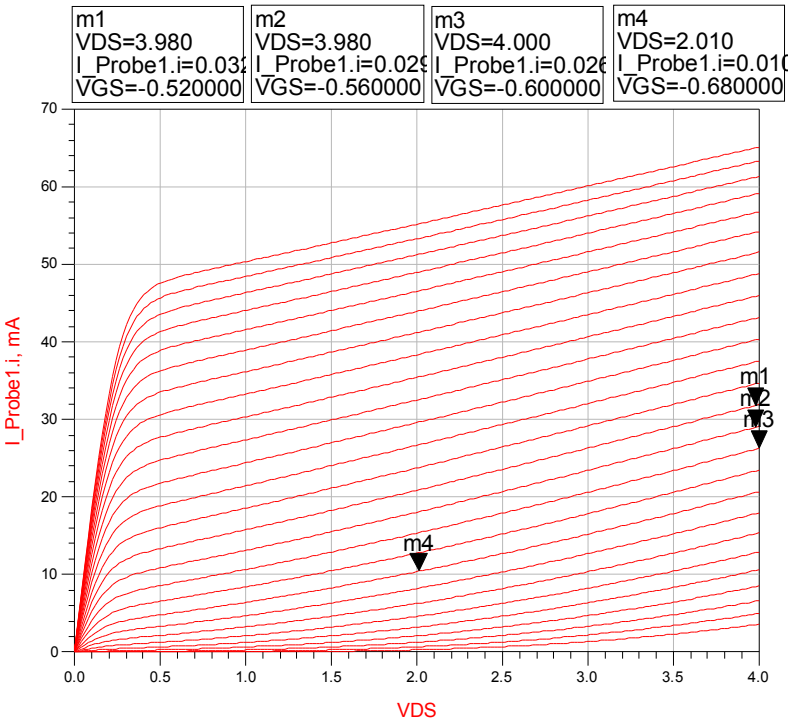
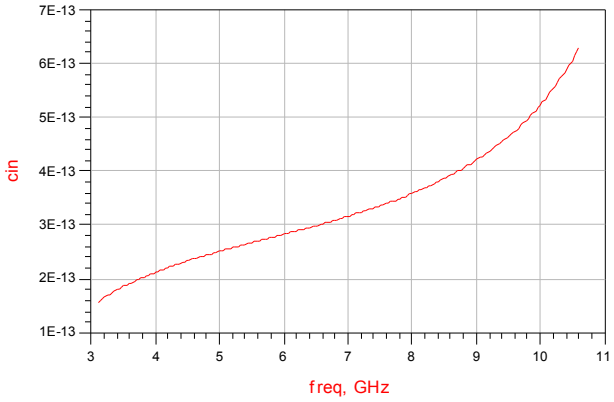


Fig 10-2: Simulated DC-IV Curve

Appendix E – C_{in} and C_{out}

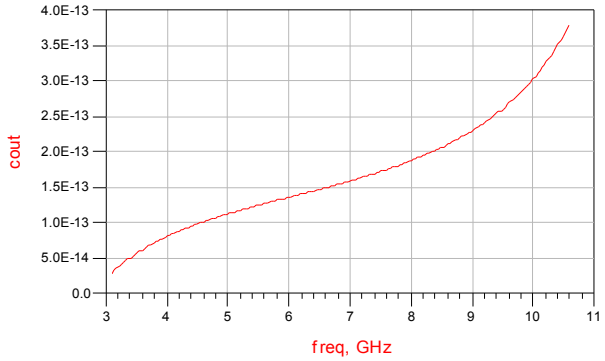
Eqn cin=imag(Y(1,1))/(2*pi*freq)



Eqn cinavg=mean(cin)

cinavg
3.338E-13

Eqn cout=imag(Y(2,2))/(2*pi*freq)



Eqn coutavg=mean(cout)

coutavg
1.686E-13

Fig 11-: Simulated C_{in} and C_{out}

Appendix F – Design Equations

EQUATION 2: $Fc = 1/\left(\prod \sqrt{L * C}\right)$

EQUATION 3: $ImageImpedence = \sqrt{L/C}$

EQUATION 4: $L1 = m * L2$

EQUATION 5: $L2 = ((1 - m^2)2 * m) * L$ **)**

EQUATION 6: $C1 = m * C2$

EQUATION 7: $C_{in} = \mathrm{Im}aginary(Y_{11})2\prod f$

EQUATION 8: $C_{out} = \mathrm{Im}aginary(Y_{22})2\prod f$

EQUATION 9: $C_d = (C - C_{out})$

EQUATION 10: $C_g = (C - C_{in})$

Standard Inductor – L
Standard Capacitor – C
Padding Capacitor in the Drain- C_d
Padding Capacitor in the Gate – C_g

Design steps for getting L, C, L1, L2, and C1

1) Solve for L in EQUATION 3.
2) Using EQUATION 2, find C.
3) Use C in EQUATION 3 to get L.
4) m = .6
5) Find L1 in EQUATION 4.
6) Find L2 in EQUATION 5.
7) Find C1 in EQUATION 6.

Appendix G – Design Task Timeline

Week of	Tasks to complete
January 25th	Lumped element models with multiple transistors and Microstrip models
February 7th	Board and inductor selections
February 14th	Test board design, fabrication, and simulations
February 21st	Test scattering parameters and compare them to simulated results.
February 28th	Design filtering system to reject outside interference
March 6th	Design filtering system to reject outside interference
March 13th	Fabrication
March 20th	Spring break
March 27th	testing of amplifier
April 3rd	testing of amplifier
April 10th	Optimization
April 17th	Optimization
April 24th	Optimization
May 1st	Project proposal and oral preparations
May 8th	Finals

References:

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