UNITRODE

U-511 Switch-Mode Power Conversion Using the bq2031

Introduction

The bq2031 incorporates the necessary PWM control circuitry to support switch-mode voltage and current regulation, as required by its charge control function block. This application note describes how to configure the bq2031 in buck mode switching power supply topology. A methodology for phase compensation of the voltage and current feedback loops is recommended. A brief description of the PWM control circuitry and phase compensation criteria appears below, followed by a discussion dealing with topology-specific issues.

The Pulse-Width Modulator

The bq2031 incorporates two voltage mode direct duty cycle Pulse-Width Modulators, one for each control loop (voltage and current). A block diagram is shown in Figure 1. Each PWM runs off a common saw-tooth waveform whose time-base is controlled by a capacitor, C_{PWM} on the TPWM pin.

The relationship of C_{PWM} to the switching frequency, FS is given by:

Equation 1

$$F_S = \frac{0.1}{C_{PWM}} \text{ kHz}$$

where:

- C_{PWM} is in µF.

The PWM for either loop consists of a comparator whose positive terminal is driven by the output of the sawtooth ramp signal, V_S, while the negative terminal is driven by the output of an Operational Transconductance Amplifier (OTA). The output is the control signal, V_C. The output of each PWM is logically ORed to generate a constant frequency pulse width modulated rectangular waveform at the MOD output. The relationship of the MOD output with respect to the OTA control signal, V_C, and the sawtooth ramp signal, V_S, is shown in Figure 2.

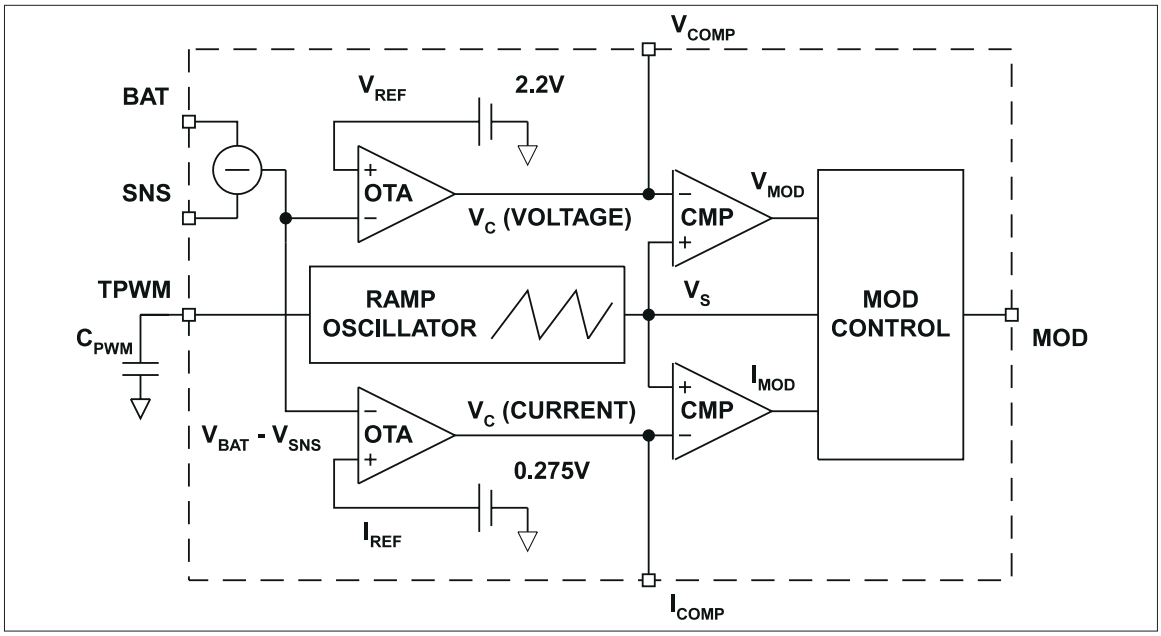

Figure 1. Block Diagram of the bq2031 PWM Control Circuitry

The MOD output swings rail-to-rail and can source and sink 10mA. It is used to control a switching transistor in a switch-mode application.

The pulse width modulated square wave signal on the MOD pin is synchronized to the internal sawtooth ramp signal. The ramp-down time (T_D) is fixed at approximately 20% of the total period (T_P). This condition limits the maximum duty-cycle to approximately 80%. For example, with a switching frequency F_S = 100kHz, T_D = 2µs.

Phase Compensation

As in any feedback control system, phase compensation is necessary to achieve both loop stability and dynamic line and load response. As shown in the PWM block diagram (Figure 1) the bq2031 provides two high-impedance nodes, I_{COMP} and V_{COMP}, for current and voltage loop phase compensation. In a battery charger application the dynamic load response is not as much a concern as loop stability, especially during voltage regulation.

Voltage and Current Control Loops

Two independent PWM function blocks implement direct duty cycle control for current and voltage regulation. During current regulation the feedback signal is the voltage across the current sense resistor, R_{SNS}, as shown in the current feedback loop model of Figure 3.

The current regulation total open-loop transfer function, IL(s), may be expressed as:

Equation 2

$$I_L(s) = A(s) * P_\omega(s) * P_T(s)$$

where:

- A(s) is OTA error amplifier and compensation network transfer function, V_C/V_O
- $P\omega(s)$ is the PWM transfer function, D/V_C
- $P_T(s)$ is the power train transfer function, $V_{O/D}$
- D is the duty cycle of the PWM waveform

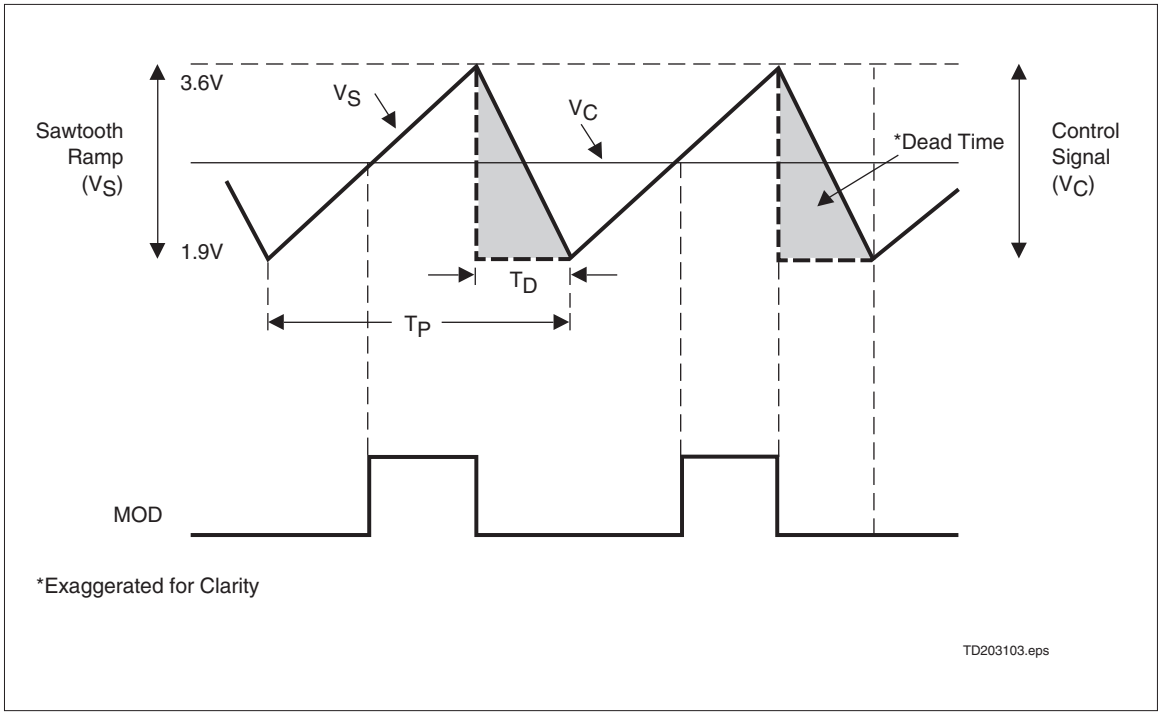

Figure 2. Relationship of MOD Output to Sawtooth Waveform V_S and Control Signal V_C

During voltage regulation, the feedback signal is the voltage sensed at the midpoint of the battery voltage divider (between RB1 and RB2). The voltage feedback control loop is modeled as shown in Figure 4.

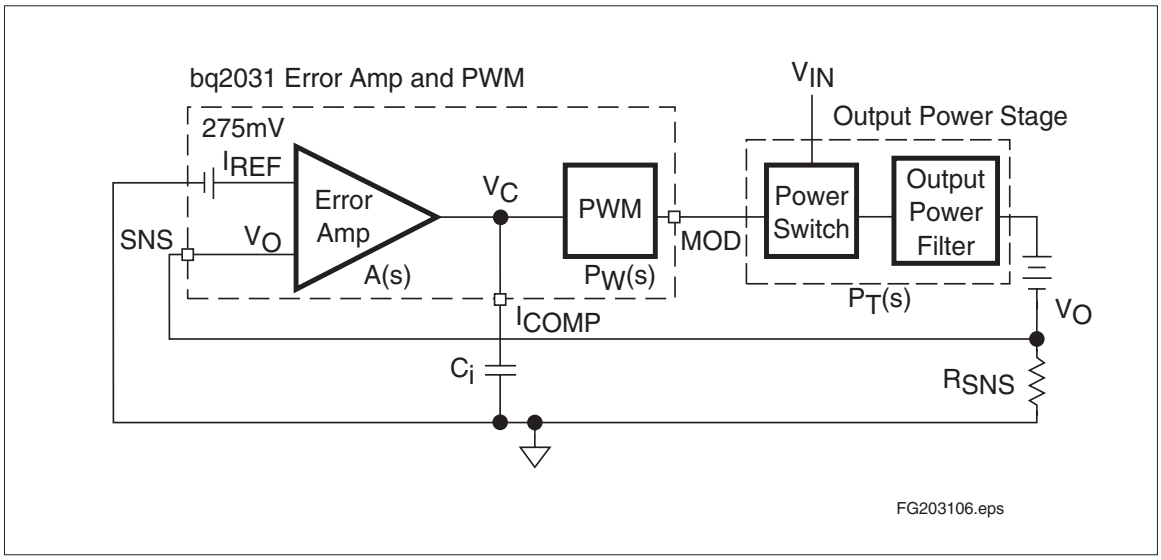

Figure 3. Model of Current Control Loop

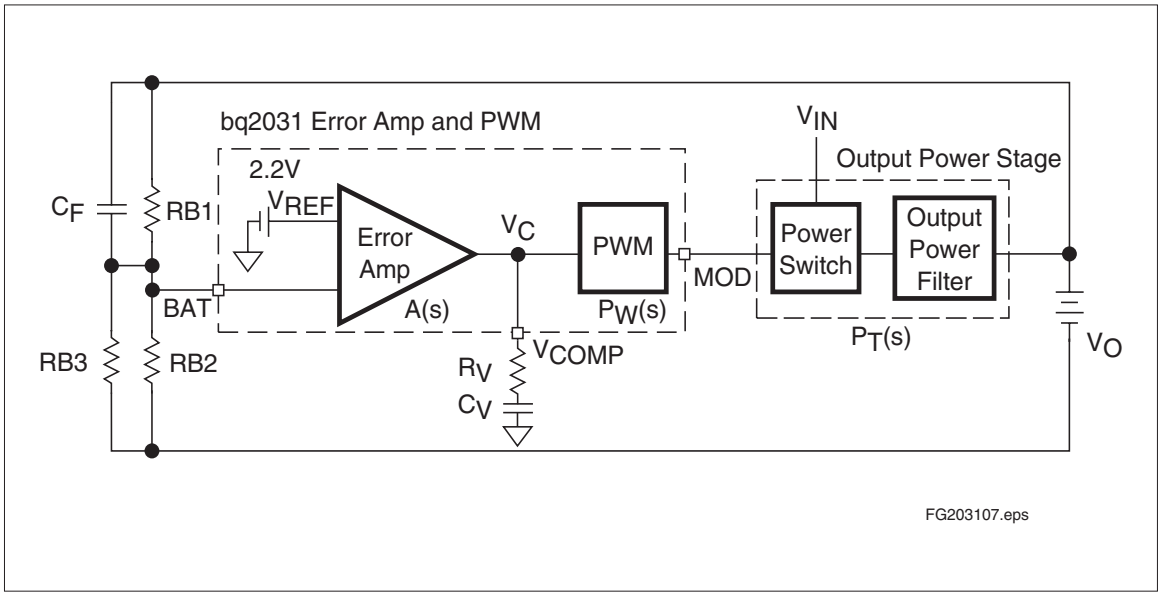

Figure 4. Model of Voltage Control Loop

For voltage regulation, the total open-loop transfer function, VL(s), may be expressed as:

Equation 3

$$V_L(s) = A(s) * P_{\varpi}(s) * P_T(s)$$

where:

- $P_T(s)$ is the transfer function of the output power stage, $V_{O/D}$.

The switching frequency and circuit topology of the system dictate the gain-frequency characteristics of the output power stage. The PWM characteristics are fixed within the bq2031. This situation leaves the OTA and its associated compensation network as the only function block whose characteristics can be changed to achieve the desired loop stability and response.

The Error Amplifier

The bq2031 error amplifiers are the OTA (Operational Transconductance Amplifier) type. The parameters of interest (see Figure 6) are:

- Transconductance gain, gm = 0.42 milli-mhos
- Output resistance of error amplifier, R = 250kΩ
- Gain Bandwidth product = 80MHz

This situation fixes the maximum voltage gain at 105 (gm*R) or 40.4dB, which is good out to the 3dB corner frequency of 2MHz. Note that the 40dB gain is the maximum achievable, regardless of the impedance across the output to ground.

Criteria for Loop Stability

The gain and phase characteristics of the OTA and associated circuitry must be adjusted to meet the following three criteria for loop stability:

1. Total open-loop gain (IL(s) and VL(s) above) must be forced to 0dB at a crossover frequency (FC) equal to at least 1/6 the switching frequency (FS).
2. The phase of the total open-loop gain at FC must be at least 45 degress less than 180 degrees.

The above criteria for loop stability can be easily achieved if the total loop-gain transfer function exhibits dominant pole characteristics as shown in Figure 5.

Stabilizing the Current Loop

From Equation 2, the total open-loop transfer function is expressed as:

$$I_L(s) = A(s) * P_{\varpi}(s) * P_T(s)$$

Pω(s) (the transfer function for the PWM) is given as:

$$P_{\varpi}(s) = \frac{D_{MAX}}{V_S}$$

where:

- D_{MAX} is the maximum duty cycle of the PWM waveform
- V_S is the peak-to-peak amplitude of the sawtooth waveform

For the bq2031, V_S is fixed at 1.7V, and the maximum duty cycle is 80%. This condition reduces the PWM transfer function to:

Equation 4

$$P_{\varpi}(s) = 0.47$$

$P_T(s)$ (the transfer function for the output power stage) is given as:

Equation 5

$$P_T(s) = \frac{V_{IN} * (1 + s * R_i * C_B) * R_{SNS}}{R_i + R_{SNS} + s[L + R_O R_L * C_B + R_{SNS} + R_i * C_B] + s^2 L * R_L * C_B}$$

where:

- s is the complex variable jω
- V_{IN} is DC input voltage
- CB is the equivalent internal battery capacitance (see Figure 11)
- L is inductor value
- R_L is inductor resistance
- R_i is the equivalent internal battery resistance (see Figure 11)
- R_{SNS} is sense resistor value
- R_O is the equivalent battery load resistance (see Figure 11)

Stabilizing the current loop requires the compensation of the loop error amplifier to be such that the transfer function A(s) has dominant pole characteristics. This can be achieved by adding a capacitor, C_i, between ground and the output of the OTA error amplier as shown in Figure 6.

The transfer function A(s) is given as :

$$A(s) = \frac{V_C}{V_O} = \frac{(g_m * R)}{(1 + (s * R * C_i))}$$

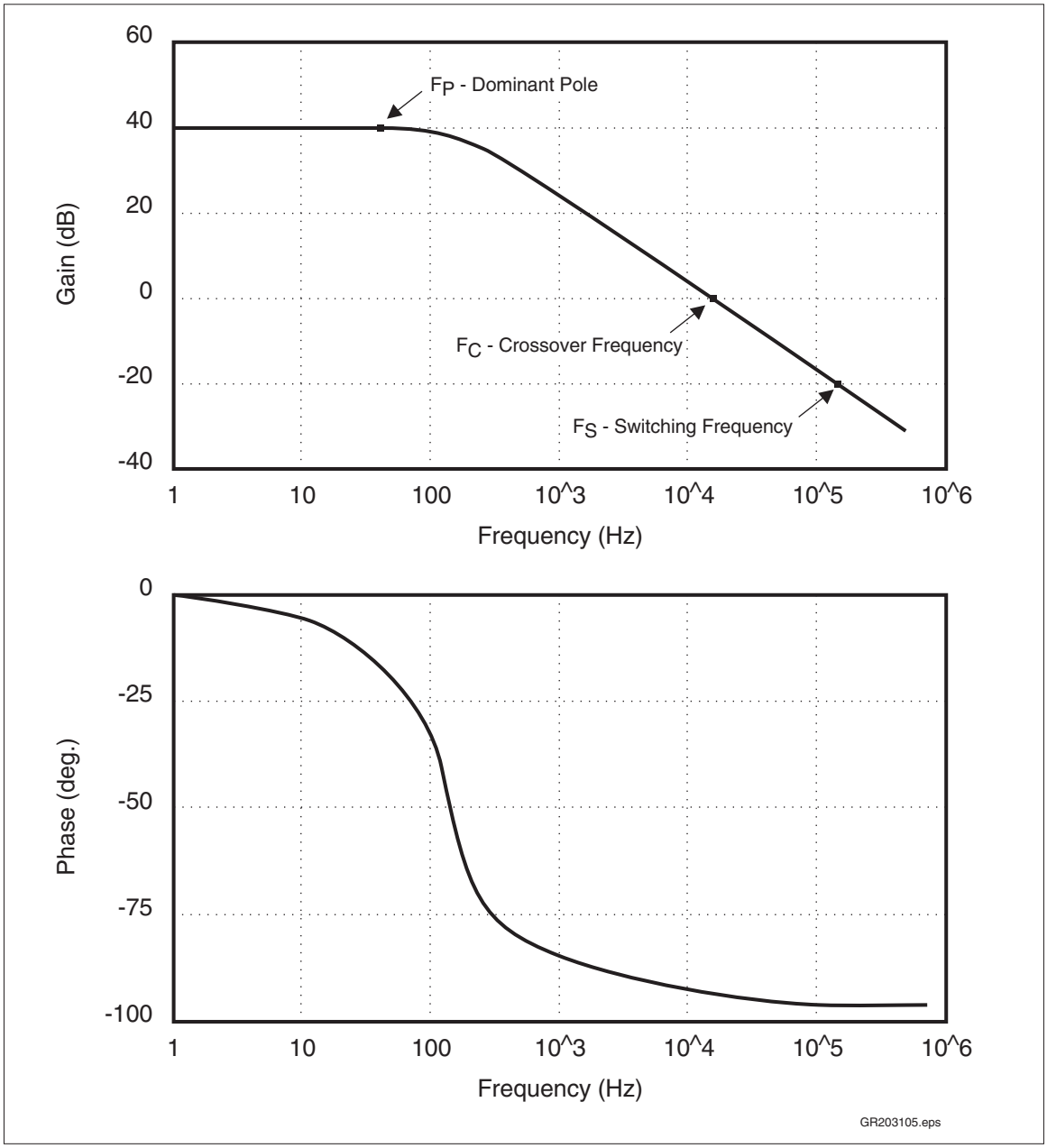

Figure 5. Target Gain and Phase Characteristics of a Stable Closed-Loop System

Substituting values for gm and R, we get:

Equation 6

$$A(s) = \frac{105}{(1 + (s * 250000 * C_i))}$$

where:

- C_i is the output capacitance of the error amplifier (see Figure 6)

Substituting Equations 4 and 5 in Equation 2 gives the compensated total current loop gain transfer function:

Equation 7

$$I_L(s) = \frac{0.47 * V_{IN} * 105}{(1 + (s * 250000 * C_i))}$$

As shown in the bode plot for IL(s) (Figure 7), C_i can be varied to achieve the necessary phase and gain margin for different V_{IN} values.

Stabilizing the Voltage Loop

Recalling Equation 3, the voltage regulation open-loop transfer function can be expressed as:

$$V_L(s) = A(s) * P_{\varpi}(s) * P_T(s)$$

The output power stage transfer function $P_T(s)$ depends on the inductor and battery impedances.

The components required to compensate the error amplifier for achieving voltage loop stability appear in Figure 8.

The resultant transfer function of the compensated error amplifier may be expressed as:

Equation 8

$$A(s) = \frac{D * 105 * (1 + s * RB1 * C_F) * (1 + (s * R_V * C_V))}{(1 + s * D * RB_1 * C_F) * (1 + s * (2.5 * 10^5 + R_V) * C_V)}$$

where:

- D = Battery voltage divider ratio during voltage regulation:

$$D = \frac{RB2 \;||\; RB3}{((RB2 \;||\; RB3) + RB1)}$$

  - **Note:** See the application note entitled "Using the bq2031 to Charge Lead-Acid Batteries" for instructions on calculating RB1, RB2, and RB3.

- RB1 = the resistor value between the high side of the battery stack and the BAT pin in the battery voltage divider network
- C_F = the capacitance in parallel with RB1
- R_V = series resistance between V_{COMP} and ground
- C_V = series capacitance between V_{COMP} and ground

(See Figure 8 and **Voltage Loop Error Amplifier Compensation** below for calculating the values of C_F, R_V, and C_V.)

The above transfer function contributes two poles and two zeros.

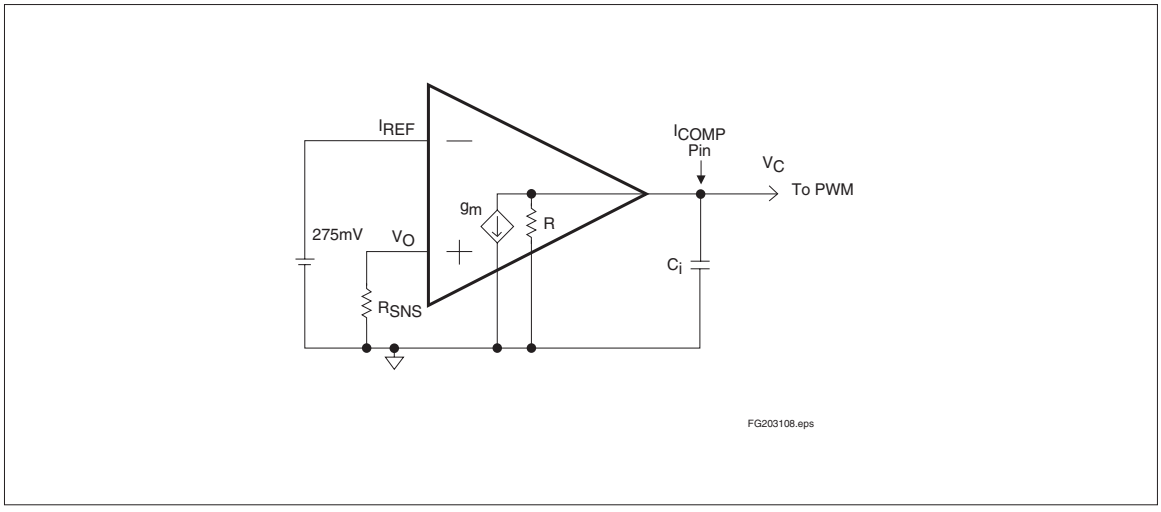

Figure 6. Compensation Network for the Current Loop

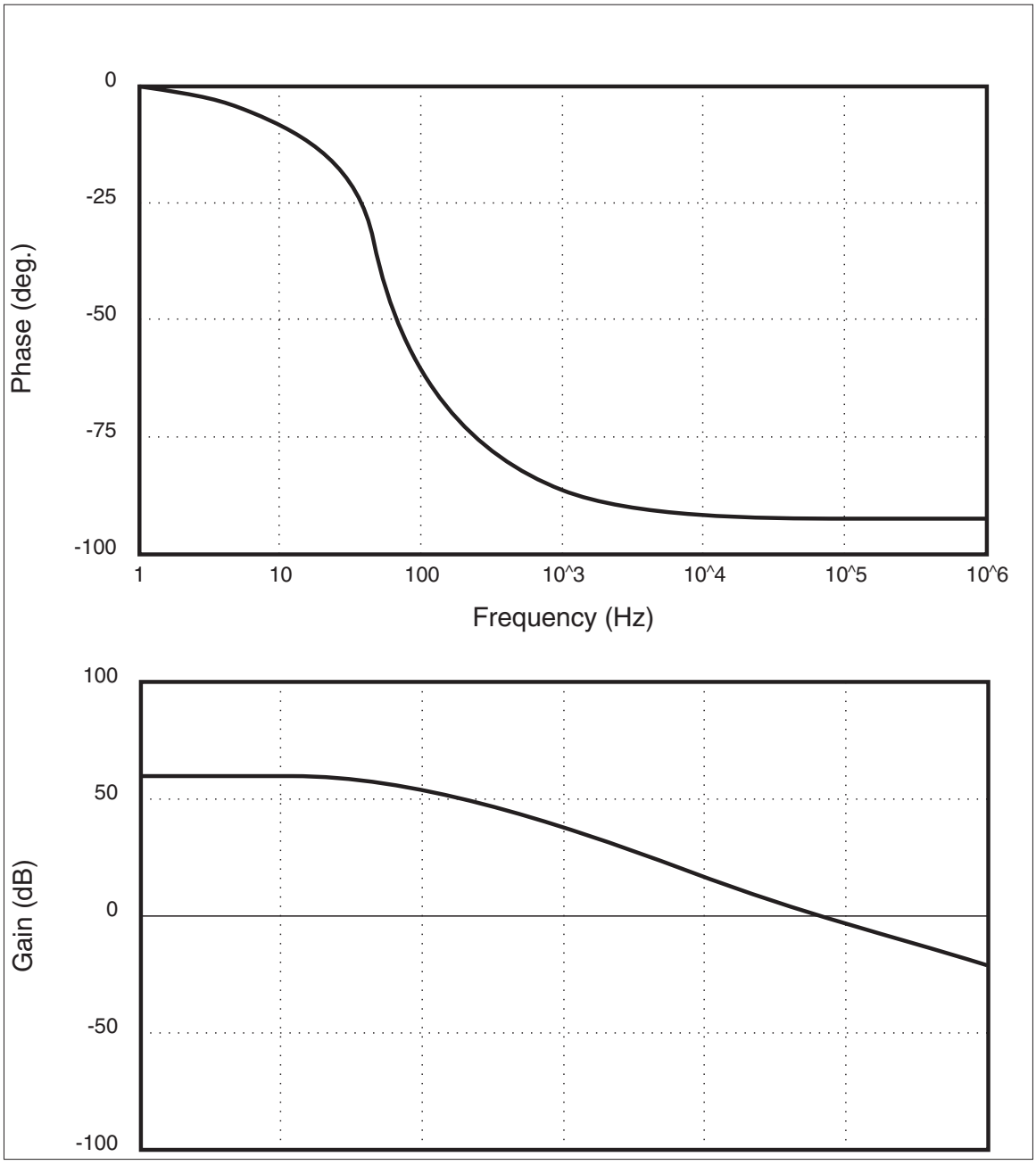

Figure 7. Bode Plot of the Current Loop-Gain Transfer Function for V_{IN} = 24V

Poles (Equation 9)

$$fp1 = \frac{1}{(2\pi * (2.5 * 10^5 + R_V) * C_V)}$$

$$fp2 = \frac{1}{(2\pi * D * RB1 * C_F)}$$

Zeros (Equation 10)

$$fz1 = \frac{1}{(2\pi * RB1 * C_F)}$$

$$fz2 = \frac{1}{(2\pi * R_V * C_V)}$$

The effect of this feedback and compensation network on the transfer function of A(s) is shown in Figure 9.

Voltage Loop Compensation for Buck Topology

Figure 10 shows a functional diagram of a switch-mode buck topology converter using the bq2031. The battery voltage is divided down to a per-cell equivalent value at the BAT pin. During voltage regulation, the voltage on the BAT pin (V_{BAT}) is regulated to the internal band-gap reference of 2.2V (with a temperature drift of -3.9mV/°C). The charge current through the inductor L is sensed across the resistor R_{SNS}. During current regulation, the bq2031 regulates the voltage on the SNS pin (V_{SNS}) to a temperature-compensated reference of 0.275V. This in turn regulates the current to I_{MAX}, provided that a properly designed resistor network is in use.

The passive component C on the I_{COMP} pin and R_V and C_V on the V_{COMP} pin form the phase compensation network for the current and voltage control loops, respectively. The diode (D_{b1}) prevents battery drain when V_{DC} is absent, while the pull-up resistor (R) detects battery removal. The resistor R13, typically a few tens of mΩ, is optional and depends on the battery impedance and the resistance of the battery leads to and from the charger board.

The Output Power Stage

The output power stage in a buck topology charger comprises the inductor L and the parallel combination of the output capacitor, Co, and impedance of the battery (see Figure 12). The output capacitor is electrolytic and in the range from 47µF to 100µF. It nullifies the inductive effect of long leads from the charger terminals to the battery.

Inductor Selection

The inductor selection criteria for a DC-DC buck converter vary depending on the charging algorithm used. For the Two-Step Current and Pulsed Current charge algorithms, the inductor equation is:

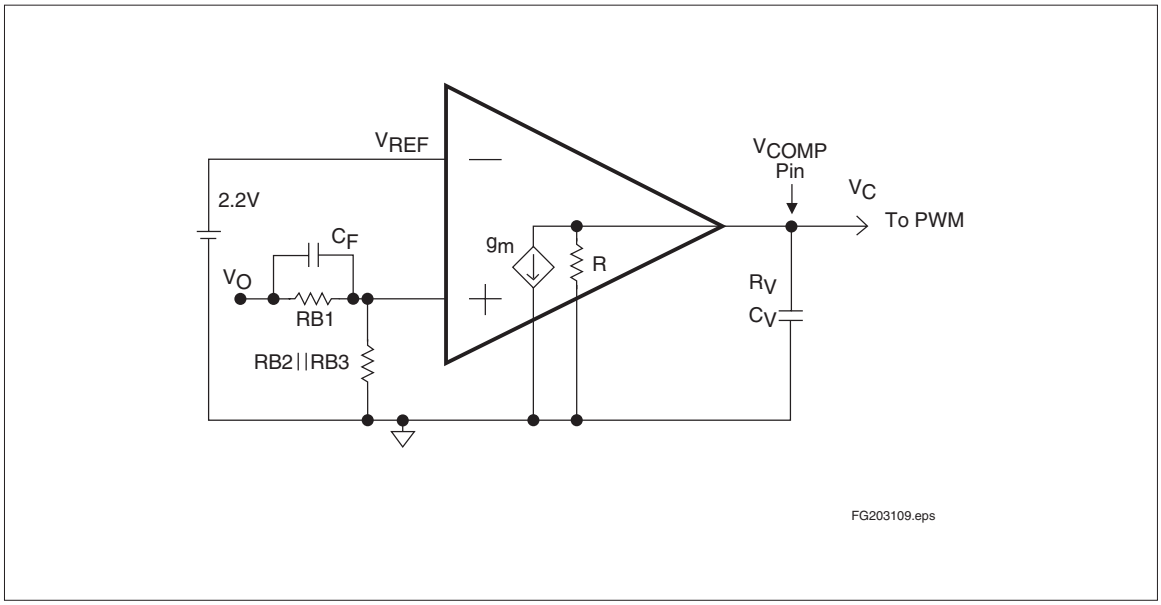

Figure 8. Compensation Network for the Voltage Loop

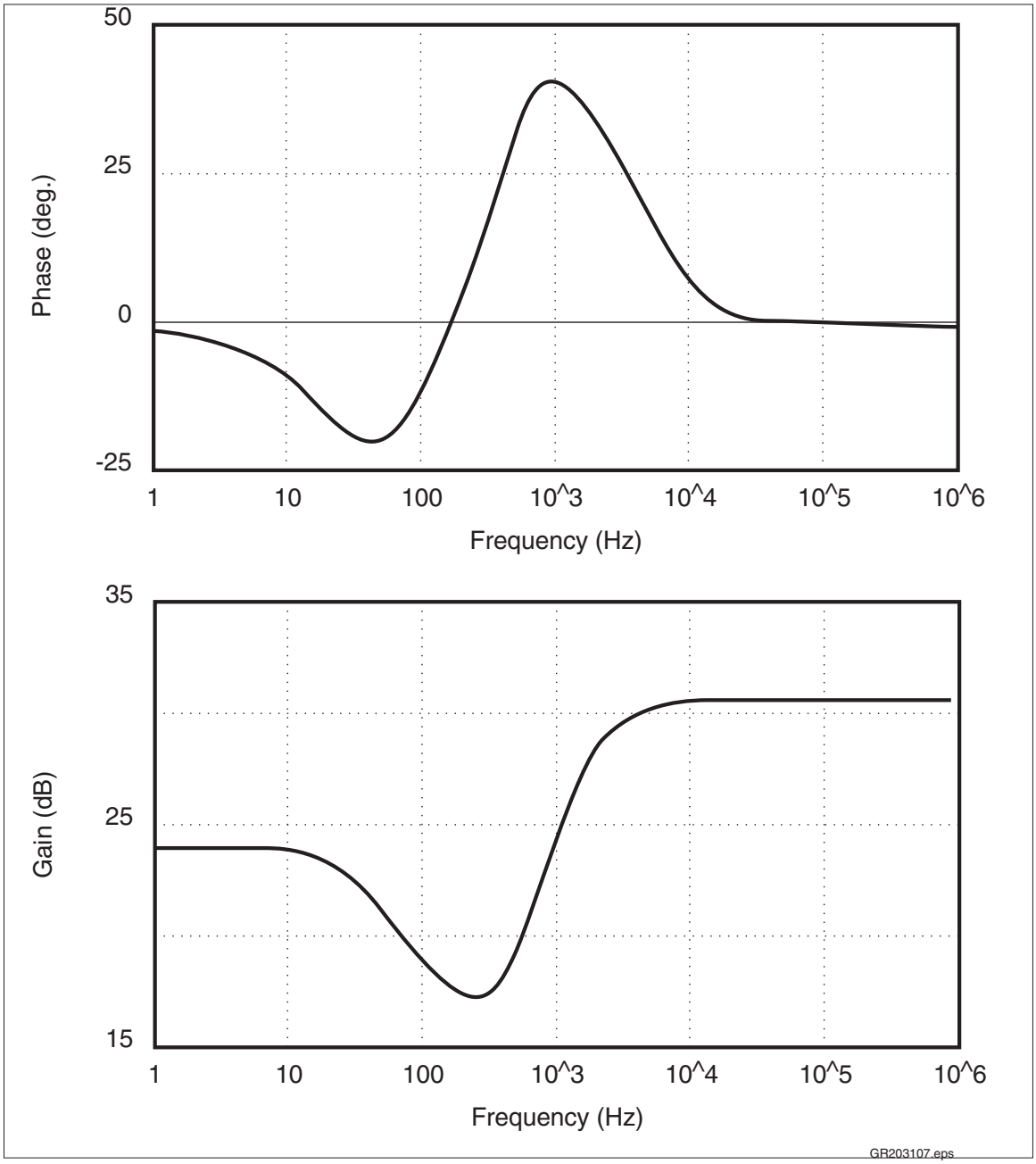

Figure 9. Effect of Compensation Network on Amplifier Transfer Function, A(s)

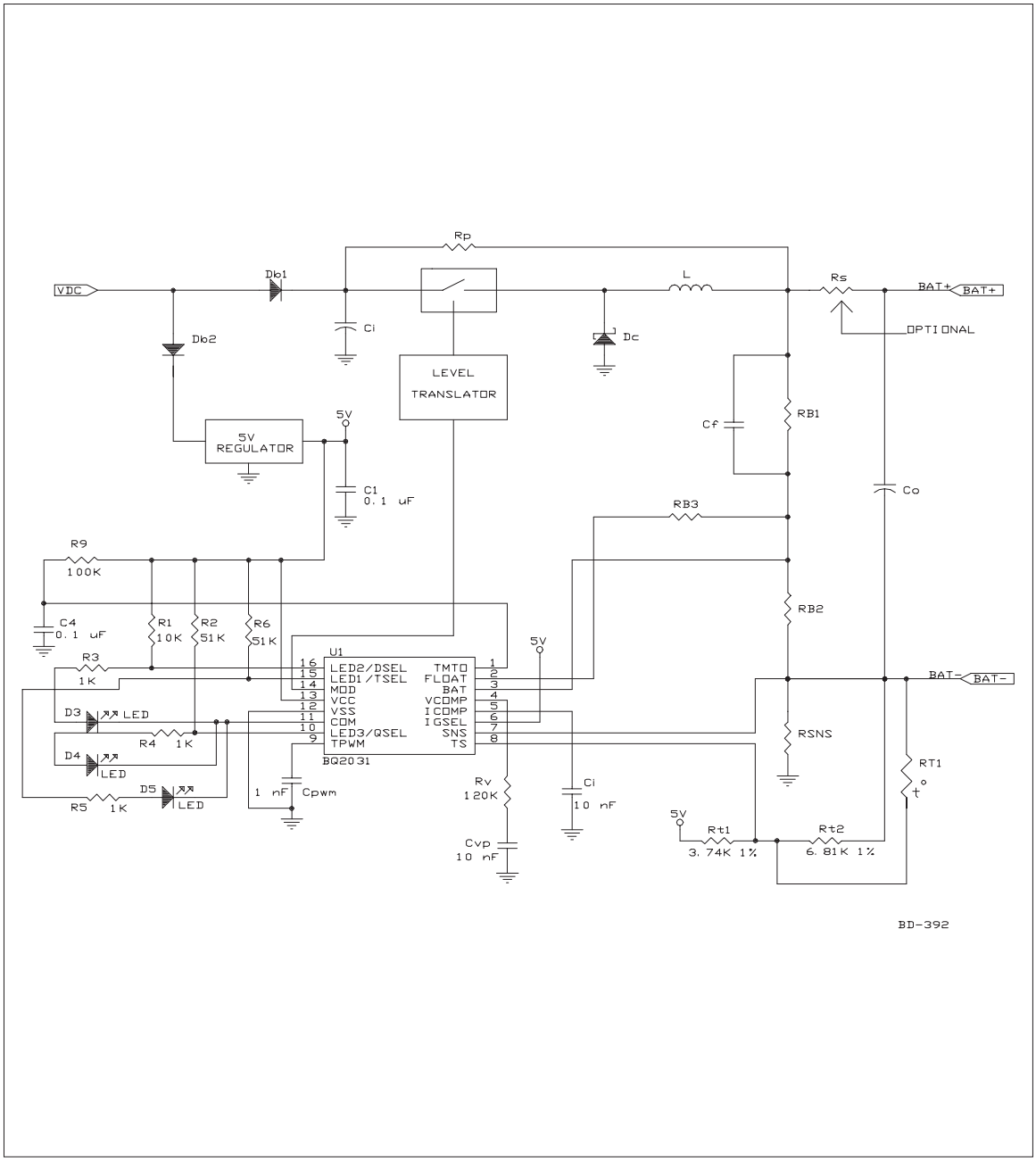

Figure 10. Functional Diagram of a Switch-Mode Buck Regulator Lead-Acid Charger Using the bq2031

Equation 11

$$L = \frac{(N * V_{BLK} * 0.5)}{F * \Delta I}$$

where:

- N = number of cells
- V_{BLK} = bulk voltage per cell, in volts
- F_S = switching frequency, in Hertz
- ΔI = ripple current at I_{MAX}, in amperes

The ripple current is usually set between 20–25% of I_{MAX}.

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Pulsed Current mode. Assuming a ripple = 25% of I_{MAX}, the inductor value required is:

$$L = \frac{(6 * 2.45 * 0.5)}{(10^5 * 0.6875)} = 107\mu H$$

The inductor current, which must remain continuous down to I_{MIN} during Fast-Charge phase 2 (voltage regulation phase), dictates the inductor formula for the Two-Step Voltage charge algorithm.

Equation 12

$$L = \frac{N * V_{BLK} * 0.5}{F_S * 2 * I_{MIN}}$$

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Two-Step Voltage mode, with I_{MIN} = $I_{MAX/20}$. The inductor value required is:

$$L = \frac{6 * 2.45 * 0.5}{(10^5 * 2 * 0.1375)} = 267\mu H$$

Model of a Lead Acid Battery

The battery impedance can be represented as a capacitor (C_B) in series with its internal impedance (R) as shown in Figure 12. The capacitance can be empirically derived from the amp-hour rating of the battery. The rule of thumb is:

$$C_B = 100 * C$$

where C = the capacity of the battery in ampere-hours.

The internal resistance Ri of a lead-acid battery is dictated by:

- Number of cells, N
- Amp-hour capacity, C
- State of charge

Figure 12 shows the variation of the internal impedance of a Yuasa NP6-12 (12V, 6 amp-hrs) battery as a function of its state of charge.

An average value of the impedance swing is recommended for use in loop stability equations. For example, with the battery above, R = 0.05Ω is recommended.

The resistor RO models the loading effects of the battery when a voltage equivalent to V_{BLK} (typically 2.45V/cell) is applied across the battery. The range of values RO takes on depends on the bulk charge current, the bulk voltage, and the I_{MIN} to I_{MAX} ratio. For example: A 12V

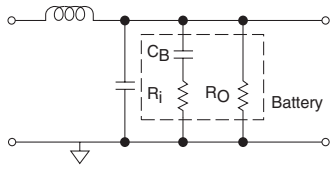

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Figure 11. Model of Output LC Filter for Buck Topology

battery being charged at I_{MAX} = 3A exhibits the following range with a I_{MIN}/I_{MAX} ratio of 1:20.

$$R_L(\min) = 6 * \frac{2.45}{3} = 4.9\Omega$$

$$R_L(\max) = 6 * \frac{2.45}{0.15} = 98\Omega$$

Use the minimum value for worst-case scenario of loop stability.

The Power Stage Transfer Function

The transfer function of the output power stage, $P_T(s)$ can be expressed as:

Equation 13

$$P_T(s) = \frac{V_{IN} * (1 + (s * R * C_B))}{(1 + (s / \omega_0)^2 + (s * (R_i C_B + L/R_O)))}$$

where:

$$\omega_0 = 1 / \sqrt{L * C_B}$$

The poles and zeros of $P_T(s)$ are:

Equation 14

$$fzo = \frac{1}{(2\pi * R_i * C_B)}$$

$$fpo = 1 / (2\pi * \sqrt{L * C_B})$$

A second pole is not used in these calculations:

$$\frac{1}{2\pi * (R_i C_B + L/R_O)}$$

Typical Switch-Mode Buck Charger Specifications

The application specifications for a switch-mode buck topology charger are usually given as :

- DC input voltage, V_{IN} = 20 to 30V
- Switching frequency, F_S = 100kHz, T = 10µs
- Charge algorithm = Two-Step Voltage mode:
  - V_{BLK} = 2.45V/cell , V_{FLT} = 2.2V/cell
  - I_{MAX} = 3A, I_{MIN} = I_{MAX}/30 = 300mA
- Battery specs: 12V, 10A-hr, Internal impedance: 0.02 to 0.07Ω

PWM and Output Power Stage Transfer Functions

Starting again from the basic voltage regulation loop-gain transfer function (Equation 3) is given as :

$$V_L(s) = A(s) * P_{\varpi}(s) * P_T(s)$$

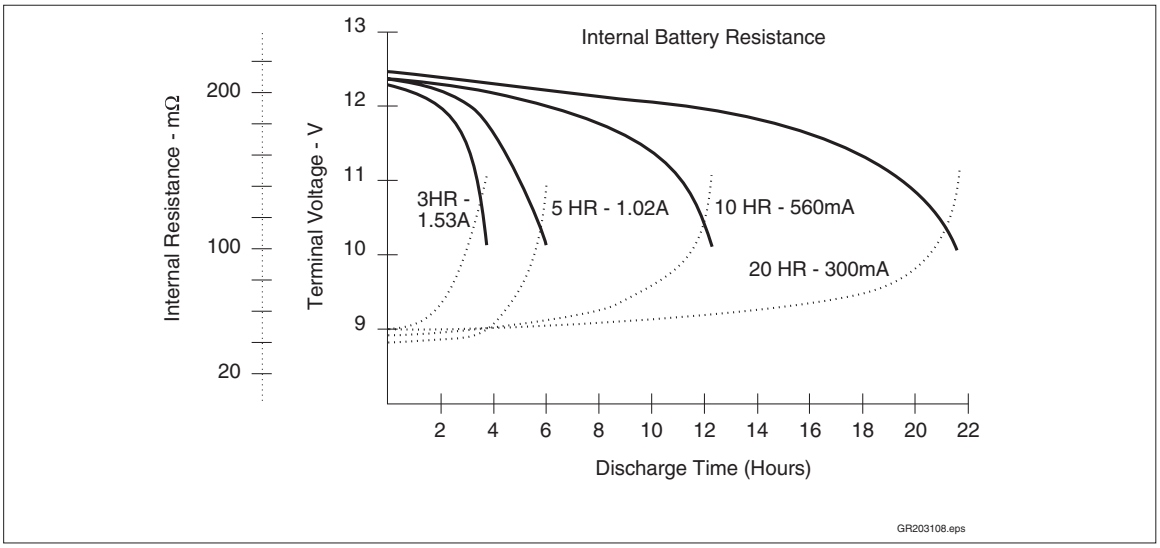

Figure 12. Internal Resistance of Yuasa NP6-12 Battery vs. State of Charge

This equation can be written as:

$$V_L(s) = A(s) * G(s)$$

where G(s) is the combined transfer function of $P_O(s)$ and $P_T(s)$

Combining Equations 4 and 13:

Equation 15

$$G(s) = \frac{0.47 * V_{IN} * (1 + (s * R * C_B))}{(1 + (s / \omega_0)^2 + (s * (R_i C_B + L/R_O)))}$$

Based on the typical values in the section above, the worst-case values for loop parameters are:

- V_{IN} = 30 V
- Ri = 0.05Ω
- $C_B = 100 * 10 = 1000\mu F$
- R_O = 4.9Ω

From Equation 12:

$$L = \frac{(6 * 2.45 * 0.5)}{(10^5 * 2 * 0.1)} = 367.5\mu H$$

The resulting bode plots for G(s) are shown below.

Since the plots exhibit similar characteristics to that of the output power filter, Equation 14 can be used to determine the poles and zeros:

- fpo = 263Hz
- fzo = 3183Hz

Voltage Loop Error Amplifier Compensation

For this control loop, appropriate values must be found for R_V and C_V, the compensation components for the V_{COMP} pin. From Table 3 of "Using the bq2031 to Charge Lead-Acid Batteries," the values for the divider network components are:

- RB1=261K
- RB2=49.9K
- RB3= 475K

Therefore

$$D = \frac{(RB2 * RB3)}{(RB2 * RB3 + (RB1 * (RB2 + RB3)))} = 0.15$$

From the first criterion for loop stability, set the crossover frequency F_C (0 dB loop-gain) to 1/20th the switching frequency:

$$F_C = F_{S/20} = 5kHz$$

Set the two zeros of A(s), fz1 and fz2, at 1/2 to cancel the second-order poles of G(s) at fpo:

$$fz1 = fz2 = fpo/2 = 263/2 = 131.5\ Hz$$

From Equation 10's first zero, fz1:

$$C_F = \frac{1}{(2\pi * RB1 * fz1)} = \frac{1}{(2\pi * 2.61 * 10^5 * 131)} = 4.63nF$$

From Equation 9's second pole, fp2:

$$fp2 = 865\ Hz$$

To achieve 0 dB loop-gain at F_C, the compensated amplifier gain at fp2 must be forced to the absolute gain of G(s) at the crossover frequency, which can be determined from the Bode plot in Figure 13 to be -31dB = 35.48.

The value for R_V can be determined from the gain magnitude equation for A(s) at fp2

$$A(f_{p2}) = \frac{105 * D * R_V}{2.5 * 10^5 * R_V}$$

Using the value of 35.48 for A(fp2) in the above equation gives:

$$R_V = \frac{35.48 * 2.5 * 10^5}{35.48 - 15.75} = 450k\Omega$$

Plugging this value for R_V into equation 10 for fz2 yields:

$$C_V = \frac{1}{2\pi * 450 * 10^3 * 131} = 2.7nF$$

Substituting these values for R_V and C_V in equation 10 for fp2 gives:

$$fp2 = \frac{1}{2\pi * (450k\Omega + (2.5 * 10^5)) * 2.7nF} = 84.2Hz$$

Figures 14 and 15 show the resultant Bode and loop gain plots for A(s), respectively.

Current Loop Error Amplifier Compensation

For this control loop, the value must be found for C_i, the compensation component for the I_{COMP} pin. The compensation network component C_i must be chosen such that the current loop gain transfer function has a dominant pole at 1/20th of the switching frequency, F(s).

$$\frac{1}{2\pi * (2.5 * 10^5) * C_i} = 131.5$$

$$C_i = \frac{1}{2\pi * (2.5 * 10^5) * 131.5} = 4.84nF$$

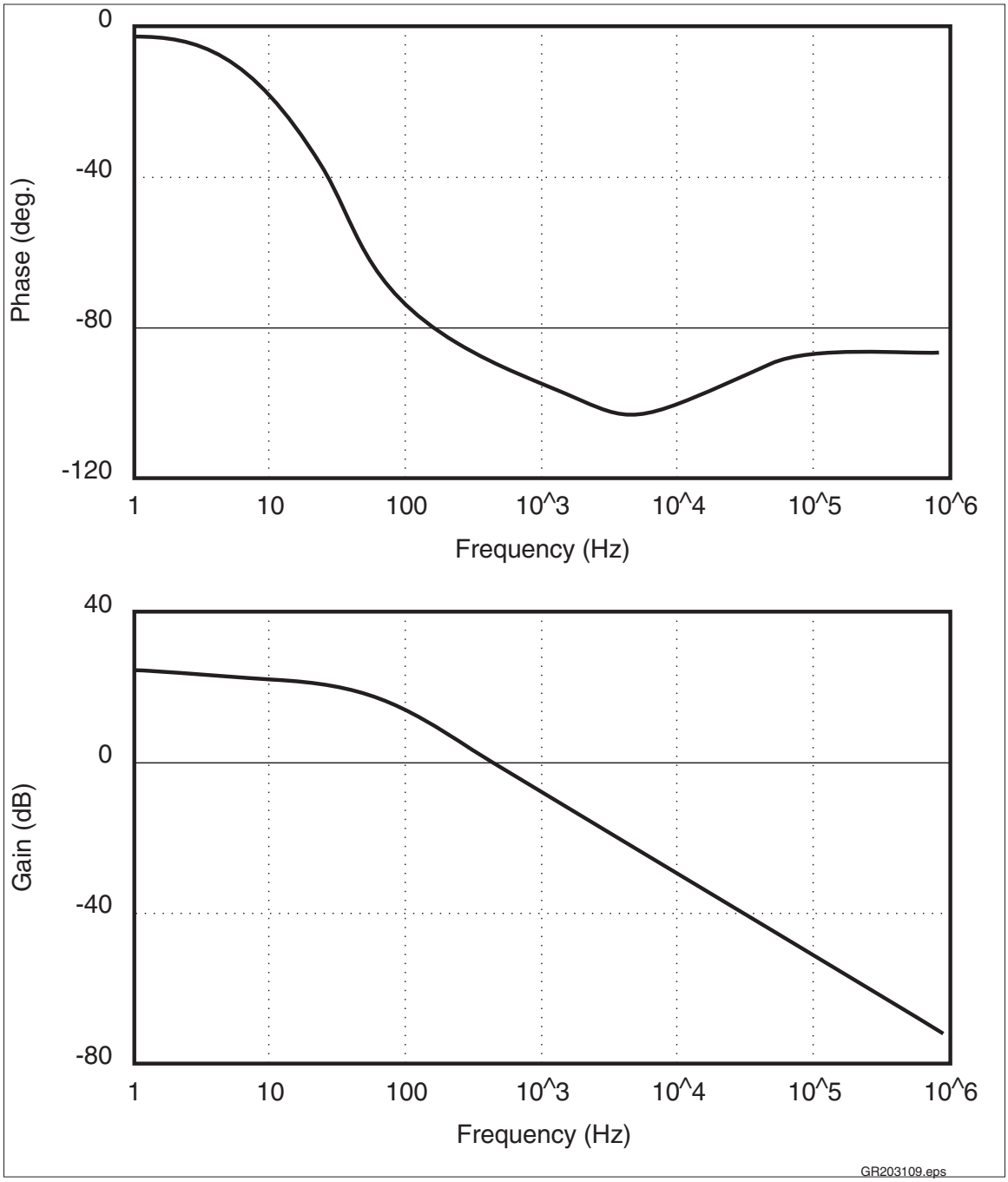

Figure 13. Bode Plot for G(s)

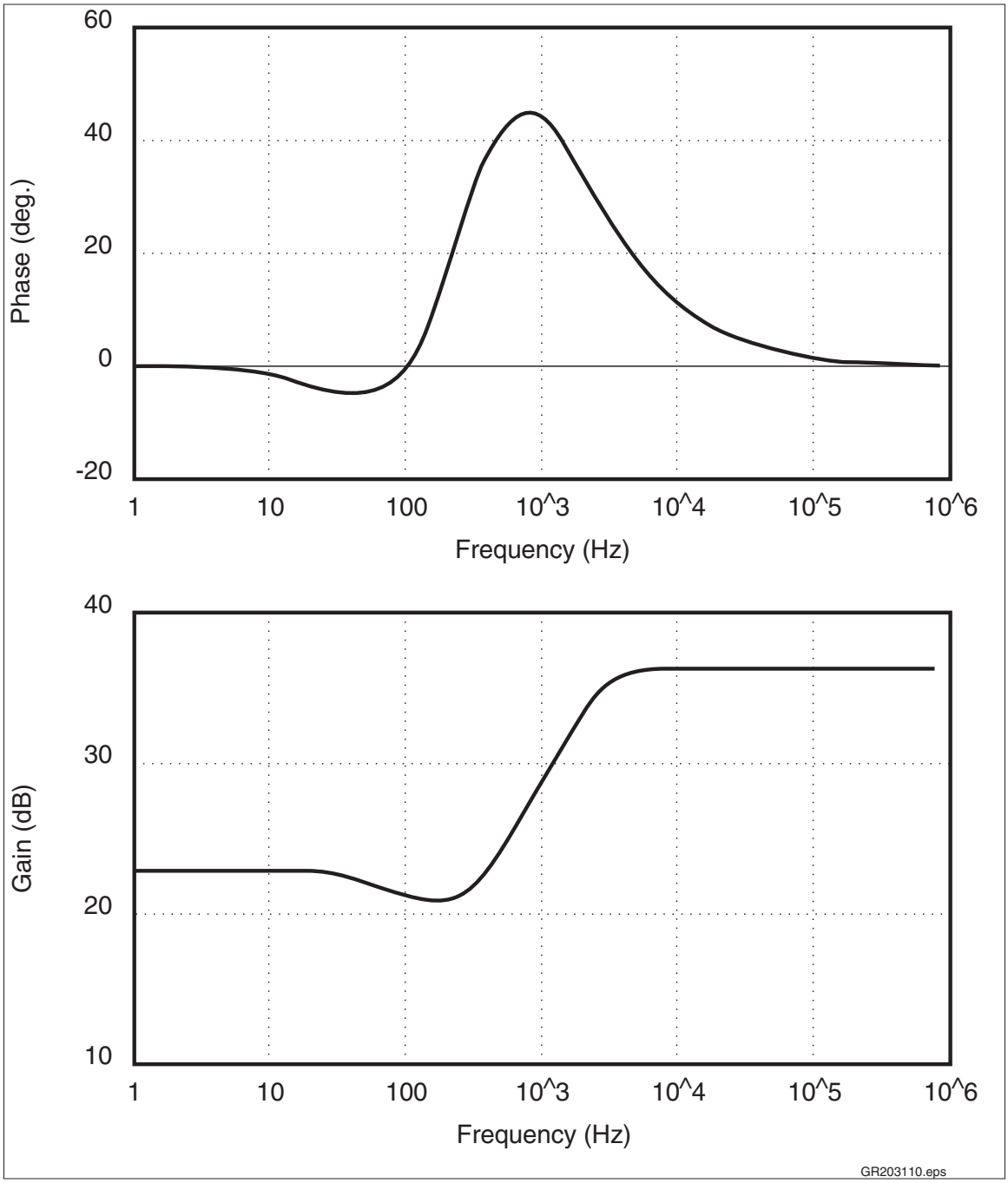

Figure 14. Bode Plot for Error Amplifier, A(s)

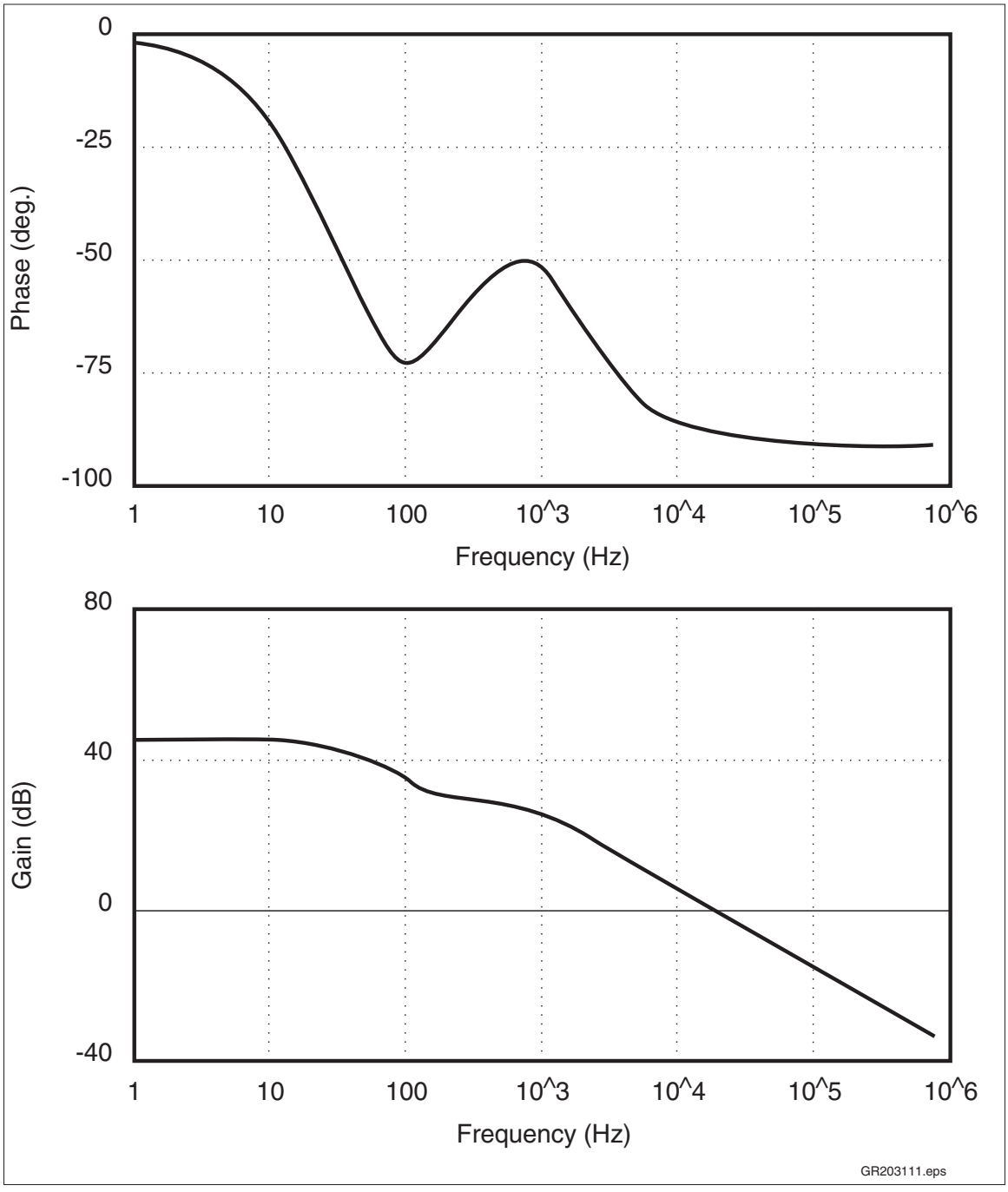

Figure 15. Loop Gain Bode/Example Buck Charger Design

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