Frequency Planning and Synthesizer Architectures for Multiband OFDM UWB Radios

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***Abstract*—This work presents an analysis on frequency planning and synthesis for multiband (MB) orthogonal frequency-division multiplexing (OFDM) ultra-wideband (UWB) radios operating in the range of 3.1–10.6 GHz. The most important specifications for the frequency synthesizer in an MB-OFDM UWB transceiver are provided. A synthesizer architecture for an existing frequency plan is introduced along with a discussion on its performance and implementation. An alternative frequency plan and its corresponding synthesizer architecture are also proposed. It is shown how this modified frequency plan leads to a significant simplification in the synthesizer realization. The feasible performance of both synthesizer architectures is evaluated through macromodel simulations using realistic models for the building blocks. Finally, system-level simulation results showing the impact of synthesizer spurs on the bit error rate performance of an MB-OFDM UWB receiver in the presence of interferers are provided. The presented results and discussion provide valuable insight for the implementation of a 3.1–10.6-GHz UWB synthesizer.**

***Index Terms*—Frequency-band plan, frequency synthesis, multiband (MB) orthogonal frequency-division multiplexing (OFDM), ultra-wideband (UWB).**

I. Introduction

DUE TO its high channel capacity, an ultra-wideband (UWB) system is an attractive solution for the implementation of very high data rate ($>$ 100 Mb/s) short-range wireless networks. Among the different options for the efficient use of the available UWB spectrum in personal computer and consumer electronic applications, the MB-OFDM approach has received strong support from several industrial organizations [1].

According to the regulations from the Federal Communications Commission (FCC), Washington, DC, UWB devices for communication applications can operate in the 3.1–10.6-GHz frequency band while employing at least 500 MHz of bandwidth (measured at -10-dB points) with a power spectral density (PSD) of less than -41.25 dBm/MHz [2]. In the multiband (MB) orthogonal frequency-division multiplexing (OFDM) proposal [3] the 7500-MHz UWB spectrum is divided into 14 bands of 528 MHz each. The bands are grouped into five band groups, as shown in the upper section of Fig. 1. Only the first band group, corresponding to the lower part of the spectrum (3.1–4.8 GHz), is considered as mandatory by the current standard proposal. The remaining band groups have been defined and left as optional to enable a structured and progressive expansion of the system capabilities. Current efforts from semiconductor companies for the implementation of UWB devices focus on the first band group to achieve a faster time-to-market and affordable power consumption with current CMOS [4] and BiCMOS [5] technologies. The realization of UWB radios for operation in the entire 3.1–10.6-GHz range is an open research area, which leads to various design challenges at both the system and circuit levels.

Fig. 2 illustrates the role of a UWB frequency synthesizer in an MB-OFDM direct conversion transceiver. As in other wireless systems, the frequency synthesizer has the crucial function of generating the local oscillator (LO) signal that drives the down-converter in the receiver path and the up-converter in the transmitter. There are at least two demanding requirements that make a frequency synthesizer for an MB-OFDM UWB radio significantly different from the widely explored synthesizers for narrow-band wireless systems, which are: 1) the range of frequencies to be generated spans several gigahertz and 2) the time to switch between different band frequencies within a band group should be less than 9.47 nS [3]. This requirement prevents the use of a standard phase-locked loop (PLL)-based synthesizer as a solution for this application [6]. Some possible ways of performing the frequency generation in a UWB device are discussed in [6]. One approach, which has been employed in [7], is to have multiple frequency sources. The synthesizer presented in [7] generates 4-, 5-, 6-, and 7-GHz tones using a single-output frequency synthesizer for each frequency. Reference [4] follows a similar approach by having three fixed-modulus PLLs; one for each of the three frequencies in band group 1. Reference [8] uses two PLLs (to generate 3960 and 528 MHz) and a single-sideband (SSB) mixer to span the frequencies in band group 1. In [9], two PLLs are again used, but this time in a different fashion to generate seven bands from 3 to 8 GHz. Reference [10] uses two frequency sources (implying two PLLs) and external inputs that are not generated within the system. It generates eight tones from 3.25 to 6.75 GHz with a spacing of 500 MHz between each tone. A more practical strategy, however, is to generate one frequency with a PLL and indirectly generate the other frequencies from auxiliary signals generated in parallel [6]. This technique is used in [1], [11], and [12]. From here onwards, the term "auxiliary signals" or "auxiliary tones"

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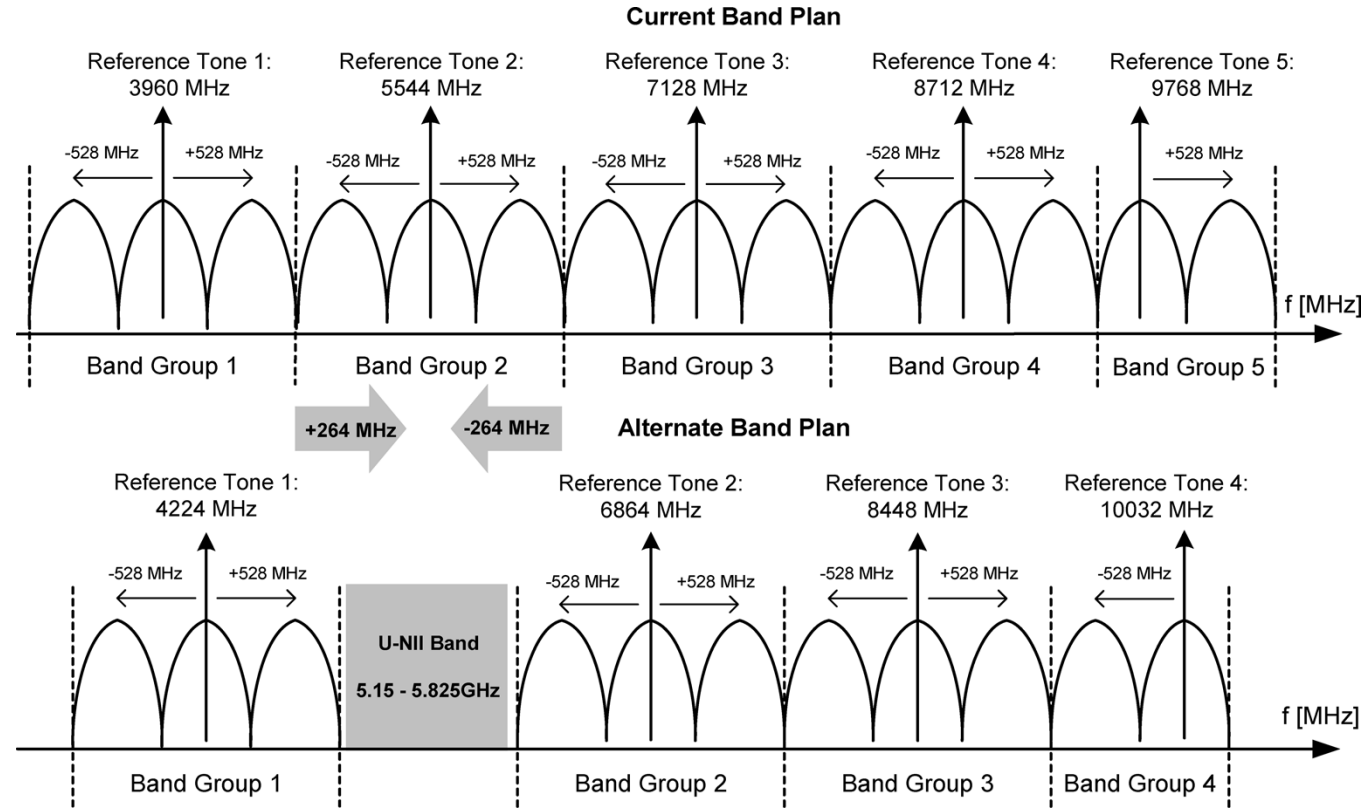

Fig. 1. Current band plan from the MB-OFDM proposal (*top*) and proposed alternate band plan (*bottom*).

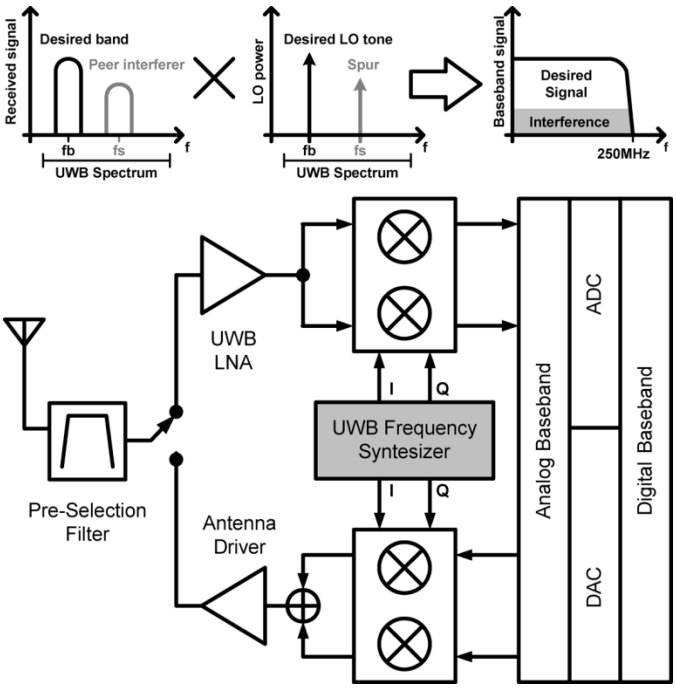

Fig. 2. Frequency synthesizer in an MB-UWB transceiver.

would refer to signals that are generated within the division loop of the PLL. Reference [11] presents a synthesizer for band group 1 based on a divide-by-7.5 structure (which uses standard dividers and SSB mixers); both the reference tone (3960 MHz) and a 528-MHz tone for up/down conversions are generated using a single PLL. The synthesizer used in [12] is based on a 16-GHz quadrature voltage-controlled oscillator (VCO), eight divide-by-2 structures, two SSB mixers, and two multiplexers to generate seven bands from 3.1 to 8.2 GHz. The diverse characteristics of the UWB synthesizers reported thus far is a clear sign of the challenge involved in the search for an optimum solution. Moreover, none of these current architectures span the entire UWB spectrum licensed by the FCC and considered by the MB-OFDM proposal. Significant research must first be performed at the system level to develop an efficient synthesizer solution (in terms of performance and power consumption) for the requirements of a completely integrated MB-OFDM UWB transceiver.

This paper addresses the problem of frequency synthesis for a 3.1–10.6-GHz MB-OFDM radio in the aspects of choice of the band plan, specifications and architecture for the synthesizer, and impact of the expected nonidealities in an integrated implementation. Section II outlines the different specifications to be met by the LO signal. Section III discusses the logic governing the frequency planning for an MB-OFDM UWB radio with a subband spacing of 528 MHz. A frequency-synthesizer architecture for the current band plan is proposed and discussed in Section IV. Section V introduces the possibility of modifying the frequency band plan to simplify the architecture of the synthesizer. Section VI presents simulation results from a macromodel of the proposed synthesizer architectures including the most important nonidealities expected in a hardware implementation. Finally, conclusions are provided in Section VII.

II. Synthesizer Specifications

In addition to the frequency switching speed, the LO signal must comply with other requirements to ensure proper operation of the MB-OFDM UWB radio. The specifications outlined here assume the OFDM parameters and bit error rate (BER) requirements described in [3] for a 480-Mb/s data transmission and an additive white Gaussian noise (AWGN) channel. A quadrature phase-shift keying (QPSK) constellation is considered for the individual sub-carriers. For a packet error rate of 8% with a 1024-byte packet, the target BER when using a coding rate $R = 3/4$ is 10^{-5}, which corresponds to an un-coded BER of approximately 10^{-2}.

A. Phase Noise

The phase noise from the LO in an OFDM receiver has two different effects on the received symbols. It introduces a phase rotation of the same magnitude in all of the sub-carriers and creates inter-carrier interference (ICI) [13]. The first undesired effect is eliminated by introducing pilot carriers with a known phase in addition to the information carriers. On the other hand, phase noise produces ICI in a similar way as adjacent-channel interference in narrow-band systems. Assuming that the data symbols on the different sub-carriers are independent, the ICI may be treated as Gaussian noise. The PSD of a locked PLL can be modeled by a Lorenzian spectrum described by

$$|\Phi(f)|^2 = \frac{1}{\pi} \cdot \frac{\beta}{f^2 + \beta^2} \tag{1}$$

where β is the 3-dB bandwidth of the PSD, which has a normalized total power of 0 dB.

The degradation (D in decibels) in the signal-to-noise ratio (SNR) of the received sub-carriers due to the phase noise of the LO in an OFDM system can be approximated as [14]

$$D \cong \frac{11}{6 \ln 10} \cdot 4\pi \cdot \beta T \cdot \frac{E_s}{N_o} \tag{2}$$

where T is the OFDM symbol length in seconds (without the cyclic extension), β defines the Lorenzian spectrum described above, and E_s/N_o is the desired SNR for the received symbols (in a linear scale, not in decibels). For this system, $1/T = 4.1254$ MHz and the E_s/N_o for the target coded BER of 10^{-5} is 5.89 (7.7 dB). For $D = 0.1$ dB and the mentioned parameters, β can be computed with (2) and is 7.7 kHz. The corresponding Lorenzian spectrum has a power of -86.5 dBc/Hz @ 1 MHz.

This phase-noise specification is to be met by the LO signal at the input of the down-conversion mixer, as shown in Fig. 2. As it will be explained in Section II-B, unlike most frequency synthesizers for narrow-band systems, a UWB synthesizer architecture involves a source PLL followed by a series of up and down conversions that will affect the phase noise of the source oscillation. For this reason, the phase-noise specification provided above does not directly correspond to the phase noise at the output of the employed source PLL. General guidelines for the analysis of phase noise in component cascades are provided in [15]. For this application, the most relevant components for phase noise degradation are the mixers employed in the frequency translation operations across the synthesizer architecture. For a given offset frequency Δf, the phase noise at the output of a mixer can be estimated as the rms sum of the individual input noise contributions. Hence, given phase-noise relative power densities $L_1\{\Delta f\}$ and $L_2\{\Delta f\}$ (in decibels relative to carrier per hertz) at the input of each port of the mixer, the output phase noise can be expressed as

$$L\{\Delta f\} = 10 \cdot \log\left(10^{(L_1\{\Delta f\}/10)} + 10^{(L_2\{\Delta f\}/10)}\right). \tag{3}$$

Even though in this case the two signals are indirectly derived from the same reference, their noise can be assumed in general to be uncorrelated since the delay from the PLL to each input of a given mixer would be significantly different. The size of an integrated implementation would be small in comparison to the wavelengths involved, but the frequency dividers and the poles in the signal path introduce a delay. As will be evident later, there is at least one frequency divider between the inputs of each mixer. The gain or loss of the mixer amplifies or attenuates all of the frequency components around the frequency of operation by the same amount and, hence, does not affect the phase noise. Moreover, due to the relatively large amplitude (tens of millivolts) of the signals within the synthesizer, the contribution of the thermal noise of the mixers to the phase noise is negligible. For a given UWB synthesizer architecture, the path with the largest number of frequency translations can be analyzed with the use of (3) to find the phase-noise specification for the source PLL.

TABLE I
Summary of Synthesizer Specifications

Band spacing	528 MHz
Switching time between adjacent bands	< 9.47 nS
Phase Noise of the LO signal	< -86.5 dBc/Hz @1 MHz
Aggregate power of spurs at band frequencies	< -24 dBc
Phase I/Q mismatch	< 5°

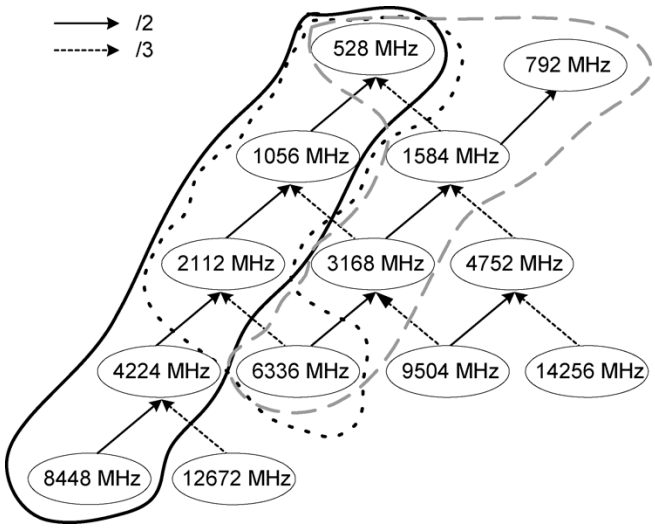

Fig. 3. Frequency tree diagram.

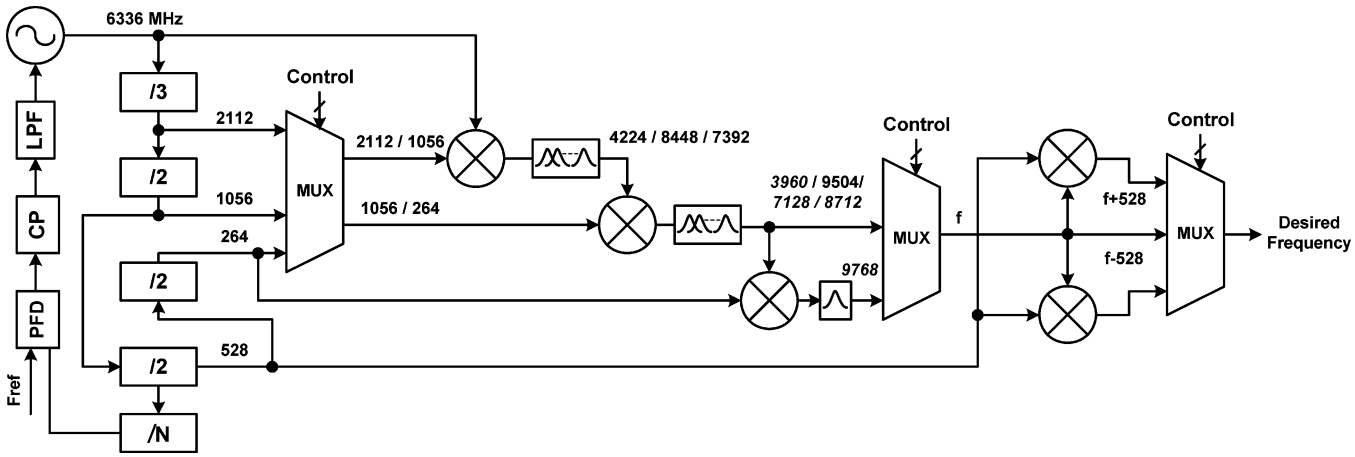

Fig. 4. Synthesizer architecture (I).

B. In-Phase (I) and Quadrature (Q) Matching

In an OFDM system, the amplitude and phase imbalance between the I and Q channels transform the received time-domain vector $\mathbf{r}$ into a corrupted vector $\mathbf{r}_{iq}$, which consists of a scaled version of the original vector combined with a term proportional to its complex conjugate $\mathbf{r}^*$. This transformation can be written as [16]

$$\mathbf{r}_{iq} = \alpha \cdot \mathbf{r} + \beta \cdot \mathbf{r}^* \tag{4}$$

where α and β are complex constants, which depend on the amount of IQ imbalance. This alteration on the received symbols can have a significant impact on the system performance. The effect of a phase mismatch in the quadrature LO signal on the BER versus SNR performance of the receiver was evaluated considering the system characteristics outlined at the beginning of this section and using a model built in SystemView [17]. Simulation results for uncoded data over an AWGN channel showed that the degradation in the sensitivity is 0.6 dB for 5° of mismatch. This degradation can be reduced with the use of coding and compensation techniques [16].

C. Spurious Content

As in other communication systems, the most harmful spurious components of an LO signal are those at an offset equal to multiples of the frequency spacing between adjacent bands (in this case, 528 MHz) since they directly down-convert the transmission of a peer device on top of the signal of interest, as shown in Fig. 2. Using the system-level model described above, it was found that, in order to have a negligible degradation in the sensitivity (< 0.1 dB); the carrier-to-interferer ratio (CIR) at baseband should be at least 24 dB. If two interferers with same power level are present, each of them must be at least 27 dB below the signal of interest. In other words, to tolerate the presence of other UWB transmissions that arrive with comparable power at the antenna of the receiver, the synthesizer spurs that appear at frequencies corresponding to other bands must have an aggregate power of less than -24 dBc. A summary of the synthesizer specifications is given in Table I.

TABLE II
SYNTHESIS OF FREQUENCIES FOR CURRENT BAND PLAN

Band #	f_o (MHz)	Frequency Synthesis
1	3432	$f_o/2 + f_o/8 - f_o/12$
2	**3960**	$f_o/2 + f_o/8$
3	4488	$f_o/2 + f_o/8 + f_o/12$
4	6600	$f_o + f_o/8 - f_o/12$
5	**7128**	$f_o + f_o/8$
6	7656	$f_o + f_o/8 + f_o/12$
7	8184	$f_o + f_o/4 + f_o/8 - f_o/12$
8	**8712**	$f_o + f_o/4 + f_o/8$
9	9240	$f_o + f_o/4 + f_o/8 + f_o/12$
10	9768	$f_o + f_o/2 + f_o/8 - f_o/12$
11	**10296**	$f_o + f_o/2 + f_o/8$

III. FREQUENCY PLANNING

The frequency-band plan introduced in [3] is shown in the upper section of Fig. 1. Each band in any band group is 528 MHz away from its adjacent band. Each band's center frequency is given by

$$f_C = (2904 + 528 \times n) \text{ MHz} \tag{5}$$

where $n = 1, 2, 3$ (band number).

The main objective of frequency planning is to maximize the number of usable bands in the available spectrum while keeping the architecture of the frequency synthesizer simple, compact, and power efficient. As mentioned in Section I, generating each band frequency using a PLL is impractical due to the very fast switching time requirement. The MB-OFDM standard proposal [3] considers that when two UWB devices communicate, they do so using the three (or two) adjacent frequencies of a band group. This implies that the synthesizer needs to hop very fast only between the frequencies of a particular band group. A relatively simple solution for the synthesis of these frequencies is to generate a reference tone (as shown in Fig. 1) for each band

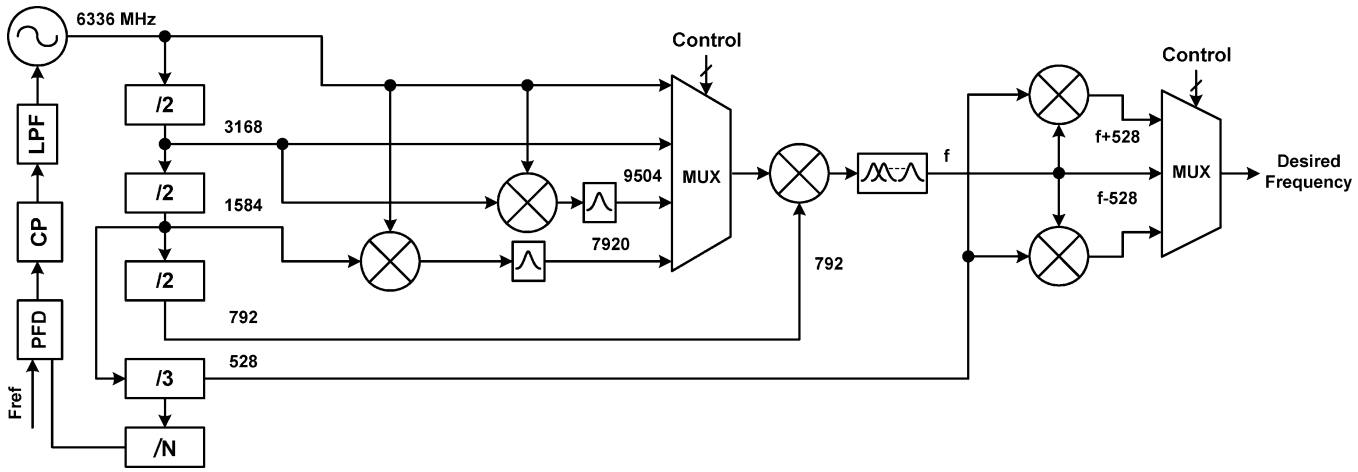

Fig. 5. Synthesizer architecture (II).

group and the adjacent frequencies through an up or down conversion by 528 MHz. A reference tone in a band group is that tone from which the required adjacent frequencies are derived.

From the above discussion, it is clear that, for the generation of any band frequency in any band group, the 528-MHz tone always needs to be available apart from the reference frequency of that band group. A very practical approach involves a PLL-based architecture where the output frequency of the PLL is fixed and the reference tones in the different band groups and the 528-MHz tone are generated (either directly or indirectly) from the auxiliary frequencies (frequencies generated in the process of deriving the PLL reference frequency from the VCO output). The auxiliary frequencies in a PLL will depend on the division ratio and the dividers used in its implementation. In order to have maximum possible auxiliary frequencies that could be derived from a fixed VCO frequency, the division ratio should be implemented with small divisors such as 2 and 3. With the assumption that a divide-by-2 and a divide-by-3 serve as the basic cells in the division loop of a PLL, a frequency tree diagram can be generated as depicted in Fig. 3. This diagram shows the different possible VCO frequencies that can result in a 528-MHz tone by successive division by 2, 3, or both. The tree also shows the different auxiliary frequencies generated in the PLL during the process of generation of the 528-MHz tone. In this way, separate synthesis of 528 MHz is avoided. The reference frequency of the PLL could be further derived from 528 MHz.

Fig. 3 provides various choices for the VCO frequency. In order to reduce the number of components and simplify the architecture, the VCO frequency should be chosen such that most of the auxiliary frequencies are the same as the reference tones. Based on Fig. 3, a band plan and a set of auxiliary frequencies can be defined to obtain an efficient synthesizer architecture.

A different, but not less important factor to consider in the choice of the frequencies to be used by the MB-OFDM UWB radio is the overlap between the Unlicensed National Information Infrastructure (U-NII) band from 5.15 to 5.825 GHz and the UWB spectrum. While the maximum output power of a UWB transmitter can reach −10 dBm when using 1584 MHz of bandwidth (three bands of 528 MHz), the devices operating in the mentioned U-NII band can have a transmit power of 16 dBm or higher. The interference from wireless local area network (WLAN) radios using the IEEE 802.11a standard are of particular concern due to their widespread use. In [3], it is estimated that an attenuation of 30 dB in the 5.15–5.825-GHz spectrum is required from a front-end filter to tolerate the presence of a 802.11a transmitter at a distance of 0.2 m. Due to the nature of their target applications, MB-OFDM and 802.11a radios will coexist in most environments preventing the effective use of a band group that overlaps with the U-NII band. For these reasons, the synthesizer architectures described in the following sections do not consider a band group in the range of 5.15–5.825 GHz.

TABLE III
SYNTHESIS OF FREQUENCIES FOR ALTERNATE BAND PLAN

Band #	f_o (MHz)	Frequency Synthesis
1	3696	$f_o/2 + f_o/16$
2	**4224**	$f_o/2$
3	4752	$f_o/2 + f_o/16$
4	6336	$f_o - f_o/8 - f_o/16 - f_o/16$
5	**6864**	$f_o - f_o/8 - f_o/16$
6	7392	$f_o - f_o/8 - f_o/16 + f_o/16$
7	7920	$f_o - f_o/16$
8	**8448**	f_o
9	8976	$f_o + f_o/16$
10	9504	$f_o + f_o/8 + f_o/16 - f_o/16$
11	**10032**	$f_o + f_o/8 + f_o/16$

IV. SYNTHESIZER ARCHITECTURE FOR CURRENT BAND PLAN

The frequency tree diagram in Fig. 3 is useful to define the architecture for the frequency synthesizer; each VCO frequency results in different auxiliary frequencies and choices for the architecture. Based on this analysis, an efficient synthesizer architecture for the existing band plan is presented here. The architecture presented in [18] for the generation of seven frequencies (between 3.432–7.920 GHz while avoiding U-NII bands) is based on a PLL that generates a tone at 6336 MHz, and is considered as a starting point for the discussion. Choosing the VCO frequency as 6336 MHz and following the path

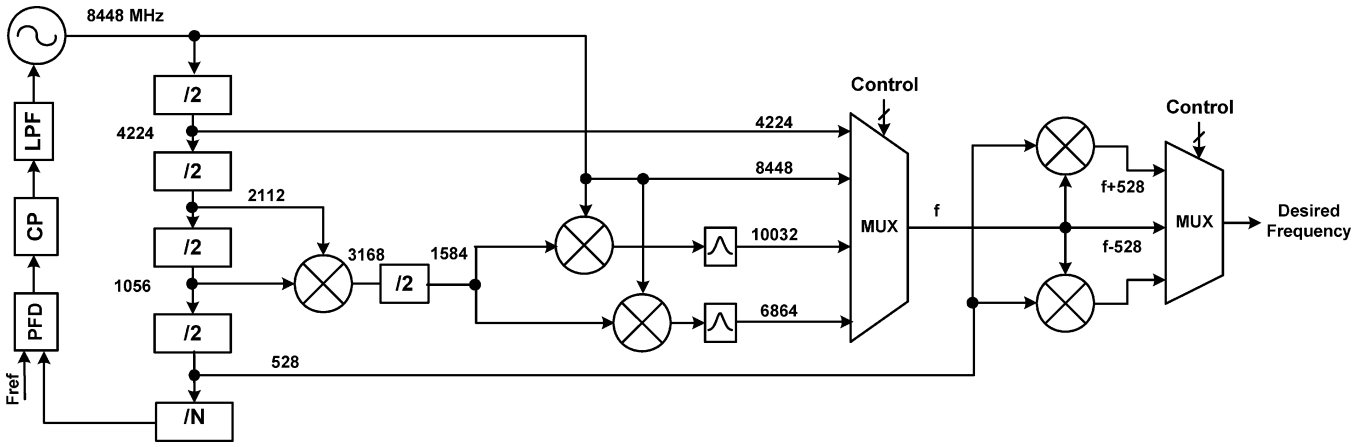

Fig. 6. Synthesizer architecture (III).

enclosed by the dotted lines (Fig. 3), a possible architecture for the current band plan can be defined as shown in Fig. 4. In contrast to the architecture in [18], this architecture generates 11 frequencies. The shaded italicized frequencies in Fig. 4 correspond to the reference tones for the current band plan shown in Fig. 1. It is important to note that the switching time between bands within a given band group depends only on the switching of the final multiplexer. This feature is shared with both of the other architectures presented below.

In this architecture option, the employed mixers need to be SSB and broad-band since they cannot be optimized for a single input or output frequency. In addition, intermediate filtering stages are required to maintain the spectral purity of the signals, which undergo a series of up/down conversions for the generation of a particular frequency. As shown in Fig. 4, one option would be to have bandpass filters at the output of such mixers, either dedicated or capable of being tuned over a wide range of frequencies. This would involve a significant amount of passives, which would increase the required area. Due to the high frequency and wide-band nature of the components involved, the power consumption of this synthesizer implementation may also become a major portion of the entire transceiver power. Hence, to obtain a suitable performance from this solution would be at the cost of significant area and power. A strategy to reduce the power and complexity in the frequency synthesizer is to identify auxiliary frequencies that can be used to generate most of the reference tones with few or no frequency translation operations. From the frequency tree diagram, it can be found that following the path enclosed within the dashed shaded line two of the frequencies, i.e., 6336 and 3168 MHz, are equally spaced (792 MHz) from their reference tones, as shown in Fig. 1. Therefore, having these frequencies at hand, one stage of mixing could be avoided in the generation of the reference tones. Based on these auxiliary frequencies, Table II shows the proposed synthesis of the reference tones for the current band plan.

A compact frequency-synthesizer architecture is proposed based on the frequency synthesis described in Table II and is shown in Fig. 5. From Table II, it can be seen that the architecture (I) was modified such that all the reference tone generations involve a final up conversion by a 792-MHz tone, which is the $f_o/8$ term in the frequency synthesis column for all frequencies. It is important to mention that the reference tone in band group 5 has changed from 9768 MHz in architecture (I) to 10 296 MHz in architecture (II).

A significant reduction in power and area would be expected due to the reduced number of mixers with multiple frequency output. However, this architecture still needs a broad-band SSB up converter for the generation of all the reference tones (up conversion with 792 MHz).

Harmonics can be curtailed by low-pass filtering at different stages, but suppressing the unwanted sidebands demands additional filtering (bandpass or band notch) for the different IFs generated in the synthesizer. In the above architecture, this would imply a wide tuning-range bandpass (or notch) filter to cater to the wide range of IFs generated (especially after the up conversion with 792 MHz) apart from the dedicated filtering wherever required (see Fig. 5). One possibility is to have dedicated SSB mixer blocks and filtering for generation of each reference tones, but that would be at the expense of higher power consumption. It must be mentioned here that the last two mixers used to generate the bands adjacent to the reference frequency (up/down conversion by 528 MHz) also have a multiple frequency input and output and would have to be broad-band. However, this structure with two mixers and one multiplexer at the end of the frequency synthesizer is common to all of the architectures presented in this work. Since filtering at the final stage would demand a broad-band tunable filter spanning several gigahertz, it is not practical and is, hence, not employed at the output of the last mixers in any of the architectures. Hence, the aim would be to have the reference frequency as spectrally pure as possible before the final up/down conversion. Therefore, an important consideration is to minimize the number of up/down-conversion operations in the generation of any reference frequency to reduce the spurs within the UWB spectrum. The above discussion highlights some of the most important considerations for the design of a frequency synthesizer in an UWB system.

V. Alternate Band Plan and Synthesizer Architecture

From the frequency tree diagram in Fig. 3, it can be noted that different sets of auxiliary frequencies can be generated in the PLL. In order to further reduce the number of multiple frequency output SSB mixers and avoid reconfigurable filtering

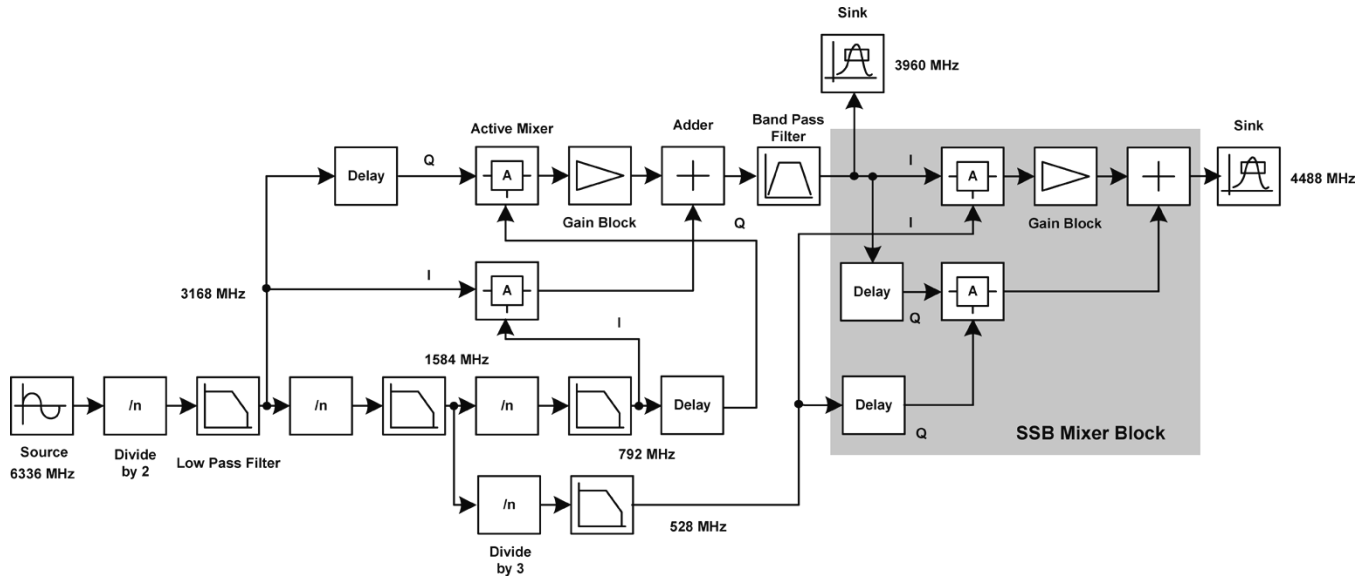

Fig. 7. SystemView setup for the macromodel.

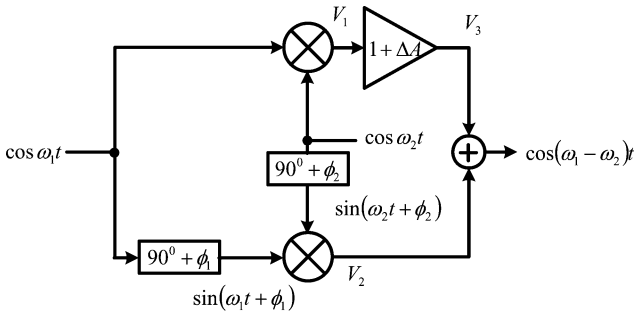

Fig. 8. SSB mixer block with phase and amplitude error. For an ideal SSB mixer, $\Delta A = 0$ and $\phi_1 = \phi_2 = 0$.

TABLE IV
DSB MIXER SPECIFICATIONS

Parameter	Specification
Conversion Gain	0 dB
RF Isolation	-30 dB
LO Leakage	-30 dB
Noise Figure	20 dB
IIP3	2 dBm

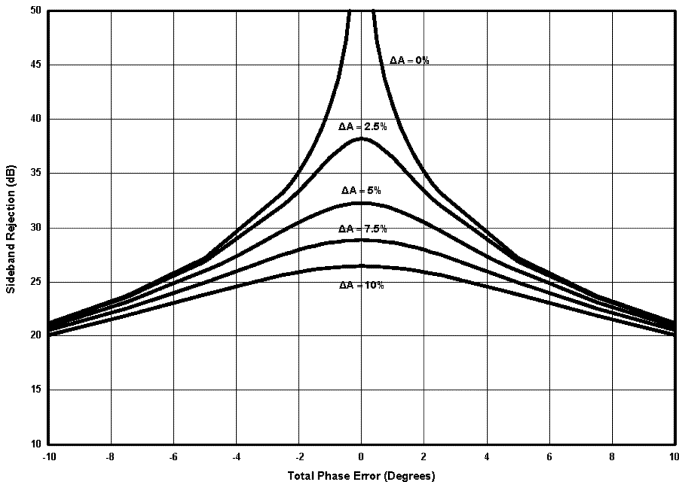

Fig. 9. Sideband rejection with amplitude and phase error.

schemes, a branch in the frequency tree can be selected such that most of the reference tones are directly generated in the divider chain (path from the selected VCO frequency to the 528-MHz tone). Looking carefully, it can be found that by moving the first three bands in band group 1 by 264 MHz to the higher side of the frequency spectrum and moving band groups 3–5 by 264 MHz to the lower side of the spectrum (as shown with gray arrows in Fig. 1), two of the reference tones (8448 and 4224 MHz) are generated in the divider chain of the PLL, which completely eliminates the need of any multiple frequency output mixer for the generation of any reference frequency. The corresponding set of auxiliary frequencies for the modified band plan is enclosed with a solid line in the frequency tree of Fig. 3. It is important to mention that this proposed modification in the band plan overlaps with the radio astronomy bands in Japan; however, it does not introduce any overlap with the U-NII band in the U.S.

Based on the frequency-generation table (Table III), a modified architecture [synthesizer architecture (III)] is proposed, as shown in Fig. 6. This architecture employs dedicated SSB mixers since each of them generates only one frequency. The most significant advantage of this architecture is that dedicated filtering can be employed at every stage wherever required to obtain a clean spectrum, thereby eliminating the need of reconfigurable filtering schemes. The generation of two reference tones within the divider chain also helps in reducing the complexity. As it will be shown in Section VI, the spurs in this architecture are diminished because of the reduced number of up/down conversions involved in the generation of the reference frequencies. In general, for an MB-OFDM UWB system, a frequency-synthesizer architecture, which minimizes the number of up/down conversions would be preferred.

TABLE V
SPURS ASSOCIATED WITH EACH BAND FREQUENCY FOR SYNTHESIZER ARCHITECTURE (II) WITH NONIDEALITIES

Band (MHz)	Generated spurs: Power in dB below the tone of interest (Spur frequency in MHz)							
3432	20.8 (4488)	21.3 (5544)	24.7 (3960)	29.8 (2640)	30.3 (4224)	31.5 (528)	31.9 (10296)	-
3960	24.3 (3168)	-	-	-	-	-	-	-
4488	20.8 (3432)	21.3 (2376)	24.6 (3960)	29.8 (3696)	30.6 (10560)	31.2 (5280)	31.5 (528)	-
6600	21.3 (7656)	21.3 (8712)	24.8 (7128)	25.4 (5808)	26.7 (7392)	30.2 (5016)	30.8 (8184)	31.5 (528)
7128	19.8 (6336)	24.8 (5544)	-	-	-	-	-	-
7656	21.3 (6600)	21.4 (5544)	24.8 (7128)	25.3 (6864)	26.8 (8448)	28 (6072)	-	31.5 (528)
8184	20.4 (9240)	21.3 (10296)	24.7 (8712)	25.6 (7392)	27.2 (8976)	27.9 (6600)	27.5 (9768)	31.5 (528)
8712	19.9 (7920)	23 (7128)	34 (5544)	-	-	-	-	-
9240	20.4 (8184)	21.3 (7128)	24.9 (8712)	25.6 (8448)	27.4 (7656)	27.1 (10032)	31.5 (528)	-
9768	23 (8184)	24.3 (10296)	25.5 (8976)	28 (10560)	31.5 (528)	-	-	-
10296	17.7 (8712)	20 (9504)	29 (7128)	-	-	-	-	-

VI. MACROMODEL SIMULATION RESULTS AND PERFORMANCE ANALYSIS

In order to obtain further insight on the performance of the proposed architectures (II and III), a macromodel was built in SystemView [17] for each of them. The models consist of divide-by-2 or divide-by-3 blocks, SSB mixer blocks composed of active mixers, low-pass filters, and bandpass filters at intermediate stages. Fig. 7 shows a block diagram of the schematic in SystemView for architecture II generating the 3960- and 4488-MHz frequencies. Since all frequencies are not available at the same time, a block diagram for the generation of all frequencies is not shown. The results presented here do not include any multiplexing. Hence, coupling and switching issues have not been considered here.

The SystemView model, as shown in Fig. 7, consists of a sinusoidal source that models the oscillator. A divide-by-N token of the communications library is used with $N = 2$ or 3 for the divide-by-2 or divide-by-3 implementation. The input to this token could be a sine or square wave, whereas the output is always a rectangular wave. The output of a divide–by-2 circuit has significant harmonic content, which results in multiple spurious tones after subsequent mixing in the later stages of the synthesizer. This is also an issue in an integrated-circuit implementation. For this reason, a first-order low-pass filter is employed at the output of each divider in the macromodel to partially filter out the harmonics. To provide additional suppression for unwanted tones (harmonics, intermodulation products, leakage, and sidebands), dedicated second-order bandpass filters are placed at the output of the SSB mixer blocks. The aim is to have as clean a signal as possible until the final up/down conversion with 528 MHz. The filters used in the macromodel are from the linear systems/filters operator group and they are of continuous time analog type. The bandpass filters used in the macromodels have a quality factor (Q) of 5, which is a realistic assumption for an implementation in current deep-submicrometer CMOS technologies.

The SSB mixers are built with the widely used configuration of two double-sideband (DSB) active mixers, as shown in Fig. 8 [19]. The active mixers used were from the RF/analog library. The specifications used for each of the DSB active mixers (in the SSB mixer) that are shown in Table IV are close to typical values provided in [20] and [21]. Whether the upper or lower sideband is rejected depends on the placement of the phase shifts or the polarity of the summing block. Since a divide-by-2 circuit can result in both I and Q signals, the divider outputs can directly form the inputs to the SSB mixer. However, in the macromodel, the quadrature signals of the divider were generated by adding a time-delay token of the delay operator group. Finally, an analysis sink was used to capture each output frequency.

Ideally, to obtain perfect rejection of one of the sidebands, the signals should be in perfect quadrature and there should be no gain mismatch in the signal paths [19]. Fig. 8 shows the SSB mixer block with the nonidealities expected from an actual circuit implementation. The sideband rejection ratio (SBRR) in an SSB mixer with a proportional amplitude error between the two DSB mixer outputs ΔA and phase errors ϕ_1 and ϕ_2 in each of the Q input signals is given by (see the Appendix)

$$\mathrm{SBRR} = 10\log\left[\frac{1+(1+\Delta A)^2+2\,(1+\Delta A)\cos\,(\phi_1-\phi_2)}{1+(1+\Delta A)^2-2\,(1+\Delta A)\cos\,(\phi_1+\phi_2)}\right]. \tag{6}$$

A plot showing the sideband rejection versus amplitude and total phase error ($\phi_1+\phi_2$) is shown in Fig. 9. For a particular case of $\Delta A = 0.05$ (5%) and $\phi_1 = \phi_2 = 5^\circ$ (corresponding to a total phase error of 10°), the sideband rejection is 20.86 dB.

Simulations are performed for architectures II and III first with the component models described above, but assuming no phase or amplitude mismatch in the SSB mixer blocks or any shift in frequencies in the intermediate filters. In this scenario, for the generation of all the required tones in both architectures, the level of each spur is at least 26 dB below the desired frequency. This could be tolerated according to the specifications outlined in Section II. From an analysis of these macromodel simulation results, it is observed that the most significant spurs are due to the finite LO leakage to the IF port since, under no amplitude or phase mismatch, the image rejection of the SSB mixer is very high. The isolation between these ports can be improved by proper circuit and layout design techniques. It must

TABLE VI
SPURS ASSOCIATED WITH EACH BAND FREQUENCY FOR SYNTHESIZER ARCHITECTURE (III) WITH NONIDEALITIES

Band (MHz)	Generated spurs: Power in dB below the tone of interest (Frequency in MHz)				
3696	20.6 (4752)	24.75 (4224)	27.9 (5808)	32.4 (528)	-
4224	-	-	-	-	-
4752	20.6 (3696)	24.75 (4224)	27.9 (2640)	32.4 (528)	-
6336	19.4 (7392)	25.5 (6864)	28 (7920)	28.3 (8448)	31.5 (528)
6864	27 (8448)	37 (10032)	-	-	-
7392	19.8 (6336)	25.5 (6864)	28 (5280)	28.5 (5808)	31.5 (528)
7920	20.6 (8976)	24.6 (8448)	27.9 (10032)	31.7 (528)	-
8448	-	-	-	-	-
8976	20.6 (7920)	24.6 (8448)	27.9 (6864)	31.7 (528)	-
9504	20 (10560)	26 (10032)	26.5 (7920)	31.5 (528)	-
10032	21.3 (8448)	34 (6864)	-	-	-

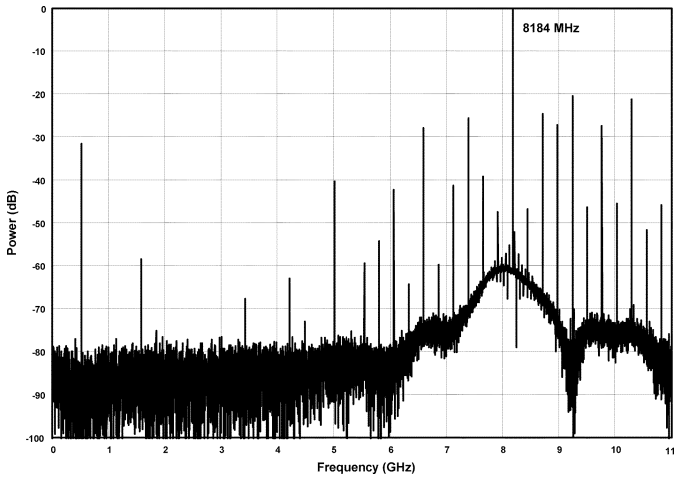

Fig. 10. Output spectrum of the synthesizer architecture (II) for the generation of the 8184-MHz tone.

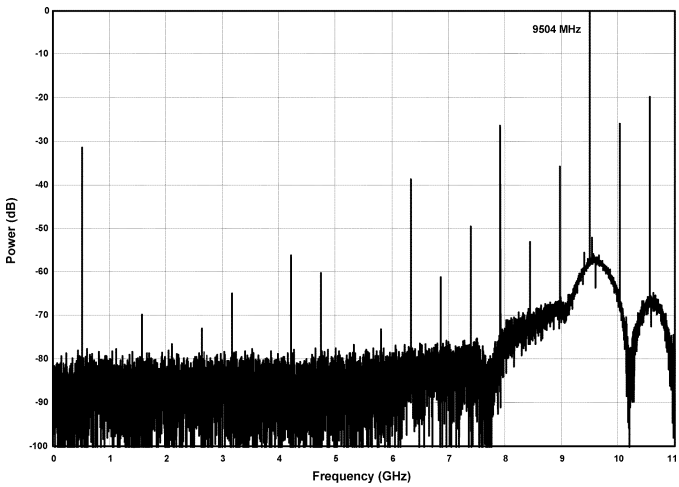

Fig. 11. Output spectrum of the synthesizer architecture (III) for the generation of the 9504-MHz tone.

be mentioned here that the LO leakage in the macromodel is implemented by a feed-forward path from the LO port adding at the output via a gain stage (with attenuation) and not through the LO leakage parameter of the model. To avoid any influence, the parameter in the model was set to a very low value. Next, simulations are performed for a worst case scenario with several nonidealities incorporated in the macromodels. These include I–Q phase mismatch (5°) in all Q paths, amplitude mismatch (5%) between the two signal paths in the SSB mixer blocks (see Fig. 8), and a frequency deviation of 10% in the center frequency of the bandpass filters. These are the most important nonidealities expected from an integrated implementation. Even though circuit implementations of frequency dividers are known to yield accurate quadrature outputs, signal routing effects such as crosstalk, loading, mismatch of parasitic components, etc. become relevant at gigahertz frequencies. For this reason, the effect of amplitude and phase mismatch for the signals across the synthesizer must be taken into account. The amplitude and phase mismatches are introduced in the macromodel by changing the gain factor of the gain block and changing the value in the delay token, respectively. It is also important to mention that the deviation considered for the center frequency

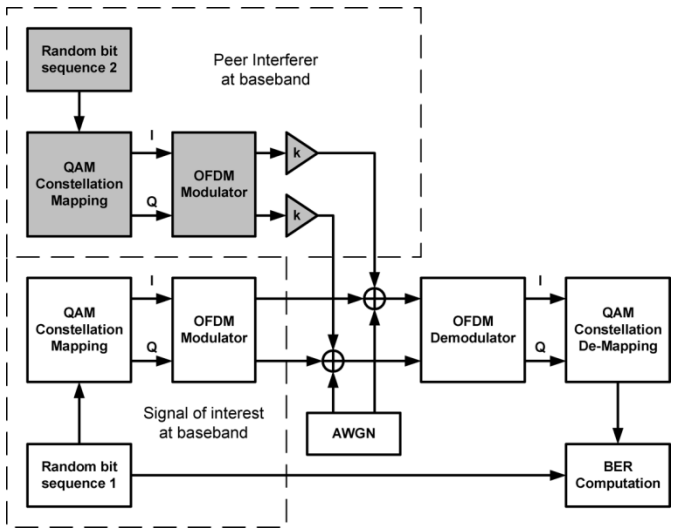

Fig. 12. Macromodel for the evaluation of the impact of the synthesizer spurs on the BER of the UWB receiver.

in each of the bandpass filters is in a way that they enhance a spur while attenuating the fundamental tone. For example, the bandpass filter centered at 3960 MHz (Fig. 7) is shifted by 10%

TABLE VII
DIFFERENT EVALUATION SCENARIOS OF BER DEGRADATION DUE TO THE INTERFERENCE FROM PEER DEVICES

Synthesizer Architecture	Band of interest (LO frequency)	Power of peer interferers in all other bands	BER Curve
II/III	Ideal case, LO signal with no spurs		a in Fig. 13, 14
II	10296	Same as band of interest	b in Fig. 13
II	8184	Same as band of interest	c in Fig. 13
II	10296	6dB above the band of interest	d in Fig. 13
II	8184	6dB above the band of interest	e in Fig. 13
III	6336	Same as band of interest	f in Fig. 14
III	8796	Same as band of interest	g in Fig. 14
III	6336	6dB above the band of interest	h in Fig. 14
III	8796	6dB above the band of interest	i in Fig. 14

to lower frequencies, i.e., toward that of the alternate sideband frequency.

Tables V and VI show the spurious tones produced during the synthesis of each of the 11 frequencies for architectures (II) and (III), respectively, in the described worst case conditions. Since in architecture (III) the 8448-MHz tone is the oscillator output and the 4224-MHz tone is generated by a divide-by-2, these tones do not create any spurious tones in the spectrum of interest and, hence, no spurs are shown for them in Table VI. It must be stressed here that because of the intermediate bandpass filters used in both the architectures, not many spurs appear in the generation of the reference tones. Figs. 10 and 11 show the output spectrum of synthesizer architecture (II) and (III), respectively, for the generation of one particular frequency. The spectrum is normalized with respect to the power of the frequency tone of interest. Fig. 10 shows the generation of the 8184-MHz tone by architecture (II). The most prominent spurious tones are at 9240, 10 296, 8712, and 7392 MHz. Likewise, Fig. 11 shows the generation of 9504-MHz tone by architecture (III), the most significant spurious tones being 10 560, 10 032, and 7920 MHz.

The spurious tones generated by the synthesizer that are outside the UWB spectrum can cause interference to other communication systems and also down-convert their emissions; thereby corrupting the received signal. The first effect must be suppressed by proper antenna design and off-chip filtering. On the other hand, if the down-converted interference from other non-UWB devices is narrow-band, it can be tolerated to a certain degree by the inherent interference rejection capabilities of the OFDM with the coded QPSK constellation modulation format employed [18]. From Tables V and VI, it can be noted that both architectures produce spurs at 5808 and 5280 MHz, which fall in the U-NII band. Architecture (II) produces a tone at 5544 MHz, which overlaps with the band used by the HIPERLAN standard. The tones at 2376 and 2640 MHz are close, but not at the populated 2.4-GHz industrial–scientific–medical (ISM) band. It is important to note that neither of the architectures produces any spur in the range of 800 MHz to 2 GHz where the mobile phone [global system for mobile communication (GSM), digital enhanced cordless telecommunications (DECT)] and global positioning system (GPS) standards are located. Moreover, the spurs generated by both architectures comply with the FCC spectral mask requirements for UWB emissions.

As shown in Fig. 2, the adverse effect of unwanted tones at frequencies within the UWB spectrum is that they down-convert the signals from peer UWB devices transmitting at the frequency of the spur, corrupting the signal from the band of interest. The impact of the synthesizer spurs on the BER of a direct-conversion receiver in the presence of other MB-OFDM UWB interferers is analyzed through a system-level model in SystemView. A conceptual description of the employed model is depicted in Fig. 12. The simulations consider the OFDM parameters described in [3] for a 480-Mb/s transmission, uncoded QPSK constellation, and AWGN channel. Under these conditions, the target BER is 10^{-2}. As shown with gray blocks in Fig. 12, in the SystemView model, each down-converted interferer is implemented with an independent random bit stream and an OFDM modulator with quadrature amplitude modulation (QAM) constellation. Before the addition to the signal of interest, each interferer is scaled by a factor k, which represents the carrier-to-interference ratio at baseband. For example, if the interferer at frequency x is received with a power 6 dB higher than the signal of interest and the synthesizer spur at frequency x has a power of -26 dBc with respect to the tone of interest, then k corresponds to -20 dB. For simplicity, only one interferer is included in Fig. 12. However, the actual simulation setup assumes that there is a UWB peer device transmitting in each of the ten bands different from the one of interest. In this pessimistic scenario, any spur from the synthesizer within the UWB spectrum down-converts an undesired peer transmission. For each architecture, a simulation is performed for the reception of each of the two bands for which the synthesizer shows the largest amount of spurs. The considered simulation scenarios are summarized in Table VII. The simulation results are shown in Figs. 13 and 14.

Two different cases are evaluated for each received band; when each of the interferers has the same power as the signal of interest and when it has 6-dB higher power. In both figures, curve "a" represents the performance of the ideal receiver with no spurs in the LO, which is also equivalent to not having any interferer. Fig. 13 depicts the receiver performance in the worst spur scenarios for architecture (II), which correspond to the re-

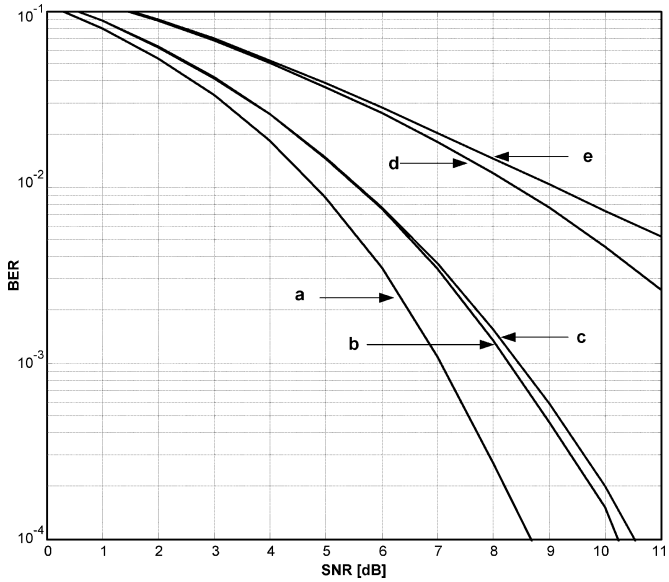

Fig. 13. BER degradation in the presence of peer interferences due to spurs in the LO from synthesizer architecture (II).

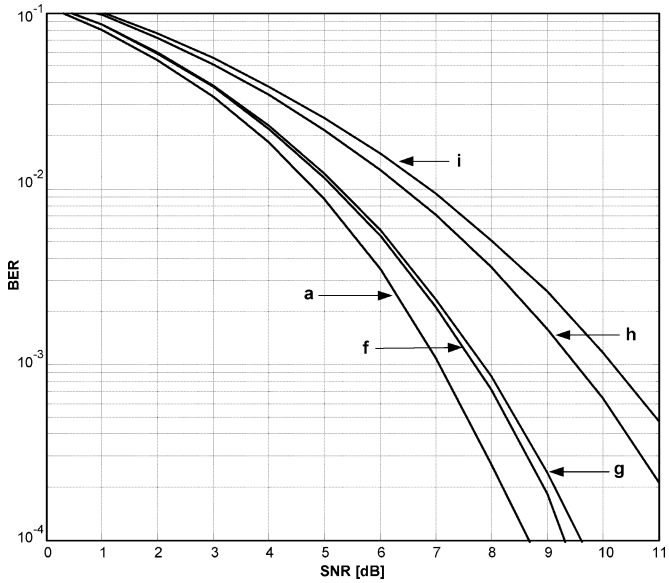

Fig. 14. BER degradation in the presence of peer interferences due to spurs in the LO from synthesizer architecture (III).

ception of the band at 10 296 MHz and the one at 8184 MHz. Fig. 14 shows the receiver performance in the worst spur scenarios for architecture (III), which are the reception of the band at 6336 MHz and the band at 8976 MHz (equivalent in terms of spurs to the reception of the 7920-MHz band). From the BER plots, it is important to observe that when the interferers have the same power as the signal of interest, the degradation in the performance is not significant ($<$ 1 dB in SNR), and the amount of spurs does not seem to make a relevant difference, i.e., the degradation is dominated by the strongest spur. However, when the power of the interferers grows, the degradation in the performance is apparently stronger for the reception cases with a larger number of spurs. It is important to mention that the bit interleaving and forward error correction techniques employed in a complete MB-OFDM radio [3] are expected to reduce the BER degradation due to interference from other UWB devices. Nevertheless, the obtained results for a pessimistic scenario with uncoded data remark upon the importance of frequency-planning and architectural design that yields the smallest amount of spurs for each generated frequency.

VII. Conclusions

The most important considerations for the selection of a band plan and the design of frequency-synthesizer architecture for an MB-OFDM radio operating in the range of 3.1–10.6 GHz have been investigated. The relationship between the choice of band frequencies and synthesizer complexity has been analyzed. Based on this study, a frequency plan has been proposed to simplify the synthesizer implementation, reduce its power consumption, and potentially improve its spurious performance. Macromodels for the two proposed architectures (corresponding to an existent band plan and the proposed one) are built considering several nonidealities from an integrated implementation and without assuming any nonconventional circuit technique. The simulation results provide significant insight for the implementation of a UWB frequency synthesizer. A detailed summary of the expected spurious components for each generated frequency has been presented and the degradation in the BER performance of the receiver due to the synthesizer spurs in the presence of UWB interferers has been evaluated. It has been seen that both architectures can tolerate certain level of nonidealities expected from a hardware implementation without compromising the receiver performance in the presence of UWB interferers with comparable power. The analysis and simulation results indicate that a proper optimization of the synthesizer architecture can result in a frequency synthesis performance suitable for the operation of an MB-OFDM radio within the UWB spectrum allocated by the FCC.

Appendix

From Fig. 8, the SBRR can be derived as follows.

The output of each mixer is given by

$$V_1 = \frac{1}{2}\left[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t\right] \tag{A.1}$$

$$V_2 = \frac{1}{2}\left[\cos\left(\omega_1 t - \omega_2 t + \phi_1 - \phi_2\right) - \cos\left(\omega_1 t + \omega_2 t + \phi_1 + \phi_2\right)\right]. \tag{A.2}$$

V_3 is a scaled version of V_1 with the amplitude error and is given by

$$V_3 = \frac{1}{2}(1 + \Delta A)\left[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t\right]. \tag{A.3}$$

Adding V_2 and V_3 at the output, we have

$$V_2 + V_3 = \frac{1}{2}(1 + \Delta A)\cos(\omega_1 - \omega_2)t + \frac{1}{2}\cos\left(\omega_1 t - \omega_2 t + \phi_1 - \phi_2\right) + \frac{1}{2}(1 + \Delta A)\cos(\omega_1 + \omega_2)t - \frac{1}{2}\cos\left(\omega_1 t + \omega_2 t + \phi_1 + \phi_2\right). \tag{A.4}$$

The fundamental tone and the sideband are given by

$$\begin{aligned} V_{\text{Fund}} &= \frac{1}{2}(1+\Delta A)\cos(\omega_1-\omega_2)t \\ &\quad + \frac{1}{2}\cos(\omega_1-\omega_2)t\cos(\phi_1-\phi_2) \\ &\quad - \frac{1}{2}\sin(\omega_1-\omega_2)t\sin(\phi_1-\phi_2) \qquad \text{(A.5)} \\ V_{\text{SB}} &= \frac{1}{2}(1+\Delta A)\cos(\omega_1+\omega_2)t \\ &\quad - \frac{1}{2}\cos(\omega_1+\omega_2)t\cos(\phi_1+\phi_2) \\ &\quad + \frac{1}{2}\sin(\omega_1+\omega_2)t\sin(\phi_1+\phi_2). \qquad \text{(A.6)} \end{aligned}$$

SBRR is a ratio of the power level of the desired (fundamental) signal to that of the sideband and, hence, only the power of the signals at the fundamental and the sideband is required as follows:

$$\begin{aligned} |V_{\text{Fund}}|^2 &= \frac{1}{4}\Big\{\big[(1+\Delta A)+\cos(\phi_1-\phi_2)\big]^2 \\ &\quad + \sin^2(\phi_1-\phi_2)\Big\} \qquad \text{(A.7)} \\ |V_{\text{SB}}|^2 &= \frac{1}{4}\Big\{\big[(1+\Delta A)-\cos(\phi_1+\phi_2)\big]^2 \\ &\quad + \sin^2(\phi_1+\phi_2)\Big\}. \qquad \text{(A.8)} \end{aligned}$$

Hence, the SBRR is given by

$$\begin{aligned} \text{SBRR} &= 10\log\frac{|V_{\text{Fund}}|^2}{|V_{\text{SB}}|^2} \\ &= 10\log\left[\frac{1+(1+\Delta A)^2+2(1+\Delta A)\cos(\phi_1-\phi_2)}{1+(1+\Delta A)^2-2(1+\Delta A)\cos(\phi_1+\phi_2)}\right]. \end{aligned} \qquad \text{(A.9)}$$

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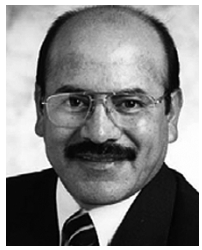
In 1992, he was with Raytheon E-Systems, Falls Church, VA, where he designed algorithms for a software-defined radio based on the Advanced Mobile Phone Service (AMPS) Standard. In 2000, he joined the Digital Signal Processing Solutions (DSPS) Research and Development Center, Texas Instruments Incorporated (TI), Dallas, TX. Since 2002, he has helped begin an internal UWB development effort within TI and co-developed the time-frequency interleaved OFDM (TFI-OFDM) proposal, which served as the foundation for the MultiBand OFDM proposal. This proposal defines a wireless UWB-based PHY for high-speed communications (up to 480 Mb/s). In addition, he serves as the PHY Technical Chair for the WiMedia/MBOA, a partnership of over 119 of the companies in the CE, PC, home entertainment, semiconductor, and digital imaging segments. In 2004, he was named one of the world's 100 Top Young Innovators by *Technology Review*, MIT's Magazine of Innovation. He is currently a Member, Group Technical Staff with TI. His research interests are in the areas of wireless communications, in particular, the design of high-speed wireless networks, multiuser detection theory, and coexistence between unlicensed wireless devices.

Dr. Batra is a member of Eta Kappa Nu and Tau Beta Pi. Since joining TI, he has also been involved in standardization activities for MBOA Special Interest Group (SIG), IEEE 802.15.3a, IEEE 802.11g, IEEE 802.15.2, and Bluetooth SIG.

Edgar Sánchez-Sinencio (F'92) was born in Mexico City, Mexico. He received the communications and electronic engineering degree (Professional degree) from the National Polytechnic Institute of Mexico, Mexico City, Mexico, in 1966, the M.S.E.E. degree from Stanford University, Stanford, CA, in 1970, and the Ph.D. degree from the University of Illinois at Urbana–Champaign, in 1973.

In 1974, he held an industrial Post-Doctoral position with the Central Research Laboratories, Nippon Electric Company Ltd., Kawasaki, Japan. From 1976 to 1983, he was the Head of the Department of Electronics at the Instituto Nacional de Astrofísica, Optica y Electrónica (INAOE), Puebla, Mexico. He was a Visiting Professor with the Department of Electrical Engineering at Texas A&M University, College Station, during the academic years of 1979–1980 and 1983–1984. He is currently the Texas Instruments Incorporated (TI), Dallas, TX, J. Kilby Chair Professor and Director of the Analog and Mixed-Signal Center at Texas A&M University. He coauthored *Switched Capacitor Circuits* (New York: Van Nostrand-Reinhold, 1984) and coedited *Low Voltage/Low-Power Integrated Circuits and Systems* (Piscataway, NJ: IEEE Press, 1999). His current interests are in the area of RF communication circuits and analog and mixed-mode circuit design.

Dr. Sánchez-Sinencio was the general chairman of the 1983 26th Midwest Symposium on Circuits and Systems (CAS). He was an associate editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (1985–1987), and an associate editor for the IEEE TRANSACTIONS ON NEURAL NETWORKS. He is the former editor-in-chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING. He is a former IEEE CAS vice president–publications. He was the IEEE CAS Society representative to the Solid-State Circuits Society (2000–2002). He was a member of the IEEE Solid-State Circuits Society Fellow Award Committee (2002–2004). He is currently a member of the IEEE CAS Society Board of Governors. In November 1995, he was awarded an Honoris Causa Doctorate by the National Institute for Astrophysics, Optics and Electronics, Puebla, Mexico, which was the first honorary degree awarded for microelectronic circuit design contributions. He was corecipient of the 1995 Guillemin-Cauer for his work on cellular networks. He was also the corecipient of the 1997 Darlington Award for his work on high-frequency filters He was the recipient of the IEEE CAS Society Golden Jubilee Medal in 1999.



Jose Silva-Martinez (SM'98) was born in Tecamachalco, Puebla, Mexico. He received the B.S. degree in electronics from the Universidad Autónoma de Puebla, Puebla, Mexico, in 1979, the M.Sc. degree from the Instituto Nacional de Astrofísica Optica y Electrónica (INAOE), Puebla, Mexico, in 1981, and the Ph.D. degree from the Katholieke Univesiteit Leuven, Leuven, Belgium, in 1992.

From 1981 to 1983, he was with the Electrical Engineering Department, INAOE, where he was involved with switched-capacitor circuit design. In 1983, he joined the Department of Electrical Engineering, Universidad Autónoma de Puebla, where he remained until 1993. He was a co-founder of the graduate program on opto-electronics in 1992. From 1985 to 1986, he was a Visiting Scholar in the Electrical Engineering Department, Texas A&M University, College Station. In 1993, he rejoined the Electronics Department, INAOE, and from May 1995 to December 1998, was the Head of the Electronics Department. He was a co-founder of the Ph.D. program on electronics in 1993. He is currently with the Department of Electrical Engineering (Analog and Mixed Signal Center) Texas A&M University, where he is an Associate Professor. His current field of research is in the design and fabrication of integrated circuits for communication and biomedical application.

Dr. Silva-Martinez has served as IEEE Circuits and Systems (CAS) Society vice president Region-9 (1997–1998) and as associate editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING (1997-1998 and 2002-2004) and for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: FUNDAMENTAL THEORY AND APPLICATIONS (since 2004). He was the main organizer of the 1998 and 1999 International IEEE-CAS Tour in region 9, and chairman of the International Workshop on Mixed-Mode Integrated Circuit Design and Applications (1997–1999). He is the inaugural holder of the Texas Instruments Incorporated (TI) Professorship-I in Analog Engineering, Texas A&M University. He was a corecipient of the 1990 European Solid-State Circuits Conference Best Paper Award.