

# **USB Logic Analyzer**

## **Functional Description**

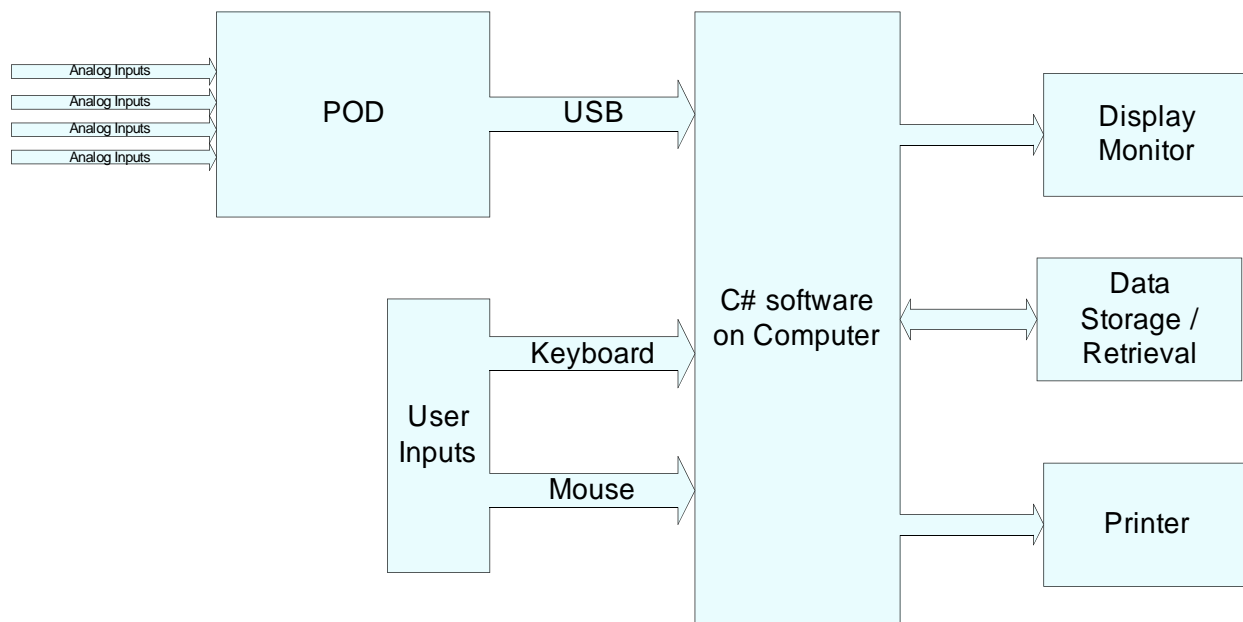
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## Introduction

A logic analyzer displays logic level of digital signals. A logic analyzer differs from an oscilloscope which is a more powerful instrument but typically only has a few channels. This project seeks to continue work on a digital logic analyzer which has sixteen channels. The logic analyzer will display four logic levels: low, high, tri-state and indeterminate. The sixteen channels are sampled by an external conditioning hardware called a POD. The POD consists of an Opal Kelly XEM 3001 FPGA board and some external hardware. The POD interfaces to the computer using Universal Serial Bus [USB] protocol. The graphical user interface [GUI] on the computer will display one of the four possible logic levels sampled by the POD. The overall system block diagram can be seen in Figure 1: Overall system block diagram for USB Logic Analyzer.



**Figure 1: Overall system block diagram for USB Logic Analyzer**

### Inputs

Analog inputs:

These are the analog voltages on the probes of the POD. The POD handles CMOS or TTL levels.

User inputs:

The user interacts with the software GUI using the keyboard and mouse, and is able to select options, change display parameters, and access additional features like zoom, scroll and save.

### Outputs

Display Monitor:

Displays the GUI. The user can see the current logic levels, triggering points and also observe the effects of their interactions with the GUI.

Data Storage/Retrieval:

Saves the captured data frame to disk. The GUI can also open and display previously saved captures.

Printer:

Prints the current screen.

## **Operation Modes**

- Option selection: Allows the user to select from the available options, such as logic type (TTL or CMOS), display window range, etc.
- Single Capture: Captures and displays information from the time the capture was started till the time software buffer was filled.
- Continuous Capture: Continuously captures information into the buffer and displays the current buffer, so the logic levels are shown at “pseudo real-time”.

## **Goals**

- Primary
  - New display engine
  - DLL interface for USB
  - Efficient data processing
  - Print/Save data capture
  - Continuous Update (Pseudo Real Time)
- Secondary
  - Remote Viewing
  - Reverse Assembly code decoding