

Altera UP2 Expansion Board

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Abstract

This project concentrates on expanding the existing laboratory digital design tools (Altera UP2/EMAC Development Kits) in the Bradley ECE Department laboratories to increase efficiency and allow for greater depth of digital design for electrical engineering students. There are several issues with the existing development kits that limit the student's ability to focus on digital design. Students must spend excessive time on labs interfacing external components which takes away from labs intended to develop digital design skills. Making mistakes is part of the learning process unfortunately with electronics making mistakes can be expensive. The Altera UP2 Expansion Board (AEB) is intended to allow students increase focus on digital design and provide protection to the existing components from potential student error.

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Introduction

The Altera University Program UP2 Kit, seen in Figure 1, is designed to help universities teach digital logic design. The package provides an Altera MAX7128S Complex Programmable Logic Device (CPLD) and an Altera FLEX10K70 Field Programmable Gate Array (FPGA) interfaced with a pair of dual 7-segment displays, 16 LED's, three DIP switches, and 4 push-buttons. While the board has proven useful in lab its potential has been very limited by the amount of lab time spent on interfacing support circuitry that is used in many applications of the board. The Altera UP2 Expansion Board will increase the students' ability to focus solely on the VHDL software design by including several commonly used components on the expansion board as well as providing protection of the existing UP2 components due to damage from student error.

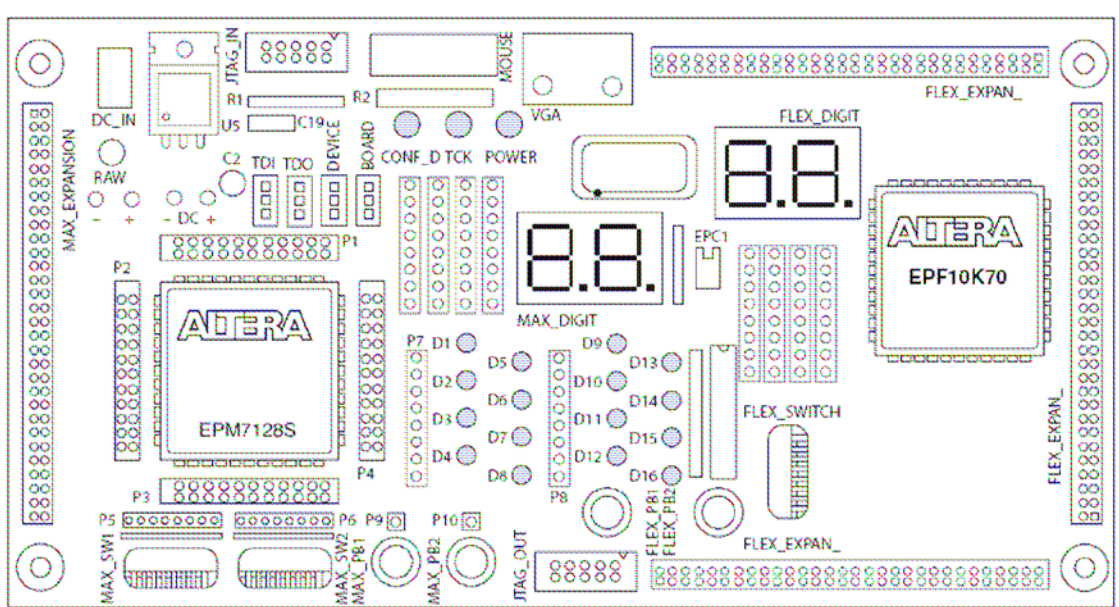


Figure 1. Altera UP2 Development Board Layout

The goal of this project was to build an Altera UP2 Education Kit expansion board (AEB) to provide a more useful test bench for complex designs. The AEB is designed for use in university laboratories by students and faculty for educational purposes. The system block diagram is shown below in Figure 2.

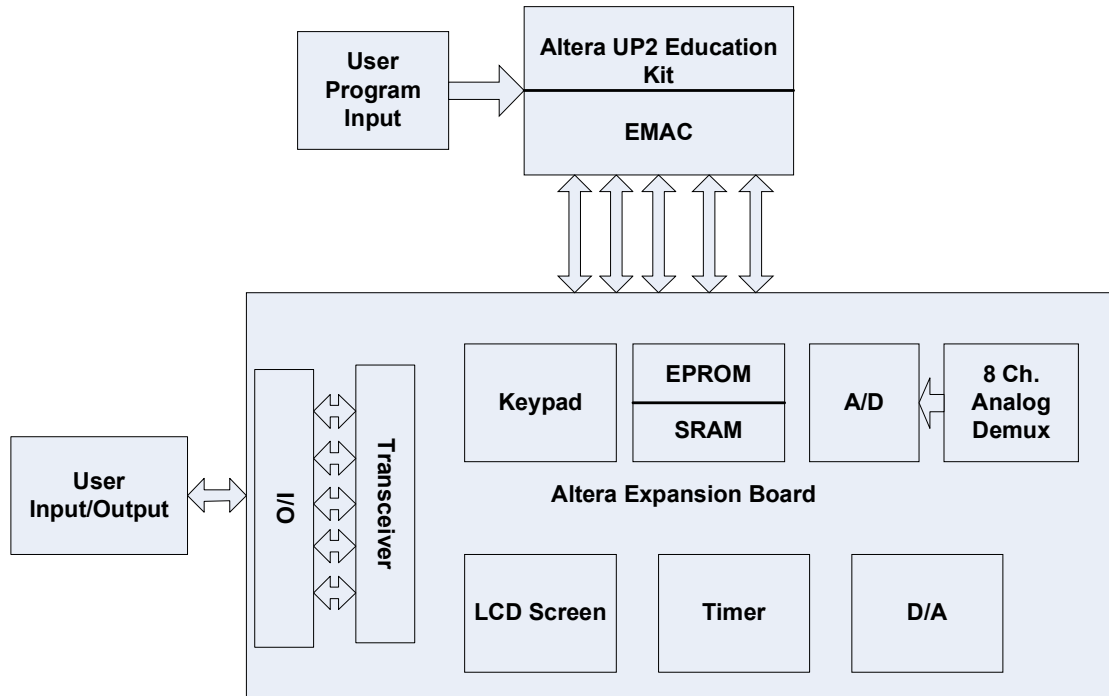


Figure 2. AEB System Block Diagram

Added Components

A listing of the added components is given below.

EPROM

The M27256 is a 262,144 bit UV erasable and electrically programmable memory (EPROM). It is organized as 32,768 words by 8 bits with an access time of 170 ns. The M27256 is housed in a 28 pin windowed Dual-in-Lin package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

SRAM

The Hitachi HM62256 is a CMOS static RAM organized as 32,768 words by 8-bits. The TTL compatible device, packaged in 600-mil plastic DIP, is available for high density mounting. It offers low power standby power dissipation.

Five Volt Voltage Regulator

The AEB uses a KA7805 3-terminal 1 ampere positive voltage regulator. The KA7805 comes in a TO-220 package and has a fixed 5V output voltage, and is capable of sourcing 1[A] of current if a proper heat sink is provided.

Programmable Timer

The Intel 8254 is a counter/timer device in a 24-pin, 600-mil ceramic Dual-in-Line package, and is designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 8254 is a superset of the 8253.

Digital-to-Analog Converter

The MAX503 is a low-power, 10-bit, voltage-output digital-to-analog converter that uses a single 5V or dual $\pm 5V$ supplies. This device has an internal voltage reference plus an output buffer amplifier. Operating current is only 250 μ A from a single 5V supply. The 10-bit resolution is achieved through laser trimming of the DAC, op amp, and reference.

Analog-to-Digital Converter

Using a modified half-flash conversion technique, the 10-bit ADC1061 CMOS analog-to-digital converter offers very fast conversion times of 1.8 microseconds maximum, yet dissipates a maximum of only 235 mW. The analog input voltage to the ADC1061 is tracked and held by an internal sampling circuit. Input signals at frequencies from DC to greater than 160 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit. For ease of interface to microprocessors, the ADC1061 has been designed to appear as a memory location or I/O port without the need for external interface logic.

Analog Demultiplexer

The CD74HCT4051 device is a digitally controlled analog switch used in conjunction with the AD1061 to provide 8 channels of analog-to-digital conversion. This analog demultiplexer controls analog voltages that may vary across the voltage supply range (i.e. VCC to VEE). They are bidirectional switches which allow any analog input to be used as an output and vice-versa. The switches have low “on” resistance and low “off” leakages. In addition, this device has an enable control which, when high, disables all switches to their “off” state.

Display and Driver

The Maxim ICM7211 four digit, seven segment display drivers include input data latches, BCD to segment decoders, and all level translation and timing circuits needed to drive non-multiplexed liquid crystal displays (LCD). The ICM7211M is the microprocessor interface version, with four BCD data inputs, two digit address lines, and two chip selects or WRITE inputs.

The Lumex LCD-S401C52TR is a four digit, seven-segment liquid crystal display. The device is 1.2 inches by 1.9 inches with characters .52 inches high.

Keypad and Encoder

The MM74C923 CMOS key encoder provides all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. This encoder also has on-chip pull-up devices which permit switches with up to 50 k Ω on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needed only a single external capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches. An internal register remembers the last key pressed even after the key is released.

Octal Transceiver

The 74HC541 are non-inverting octal buffers and line drivers with three-state outputs that can drive 15LSTTL loads. The output enables (OE1,OE2) control the tri-state outputs. If either OE1 or OE2 is high the outputs will be in the high impedance state. For data output OE1 and OE2 both must be low.

Design and Layout

Once the components had been procured, a symbolic representation of each component was created in OrCAD Capture and saved in a custom library. Each symbol contained component names, pin-names, and pin numbering. Figure 3 shows an example of some of these custom symbols. After the symbolic library was created, another custom library was created in OrCAD Layout for the footprints of each component. A footprint includes all of the physical dimensions of a component, including pin spacing and numbering. It is crucial that the pin numbering in the footprint corresponds to the same pin in its corresponding symbol. This library is shown in figure 4.

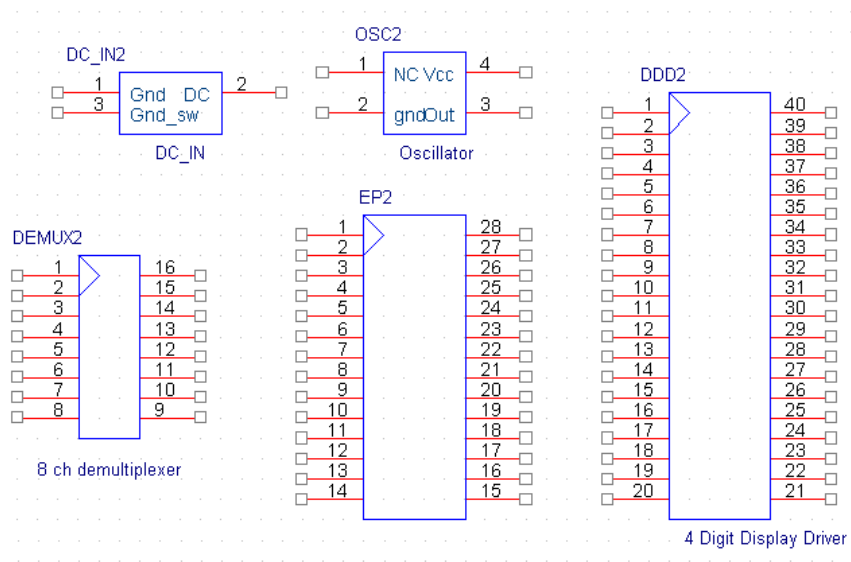


Figure 3. Component Symbols in OrCAD Capture

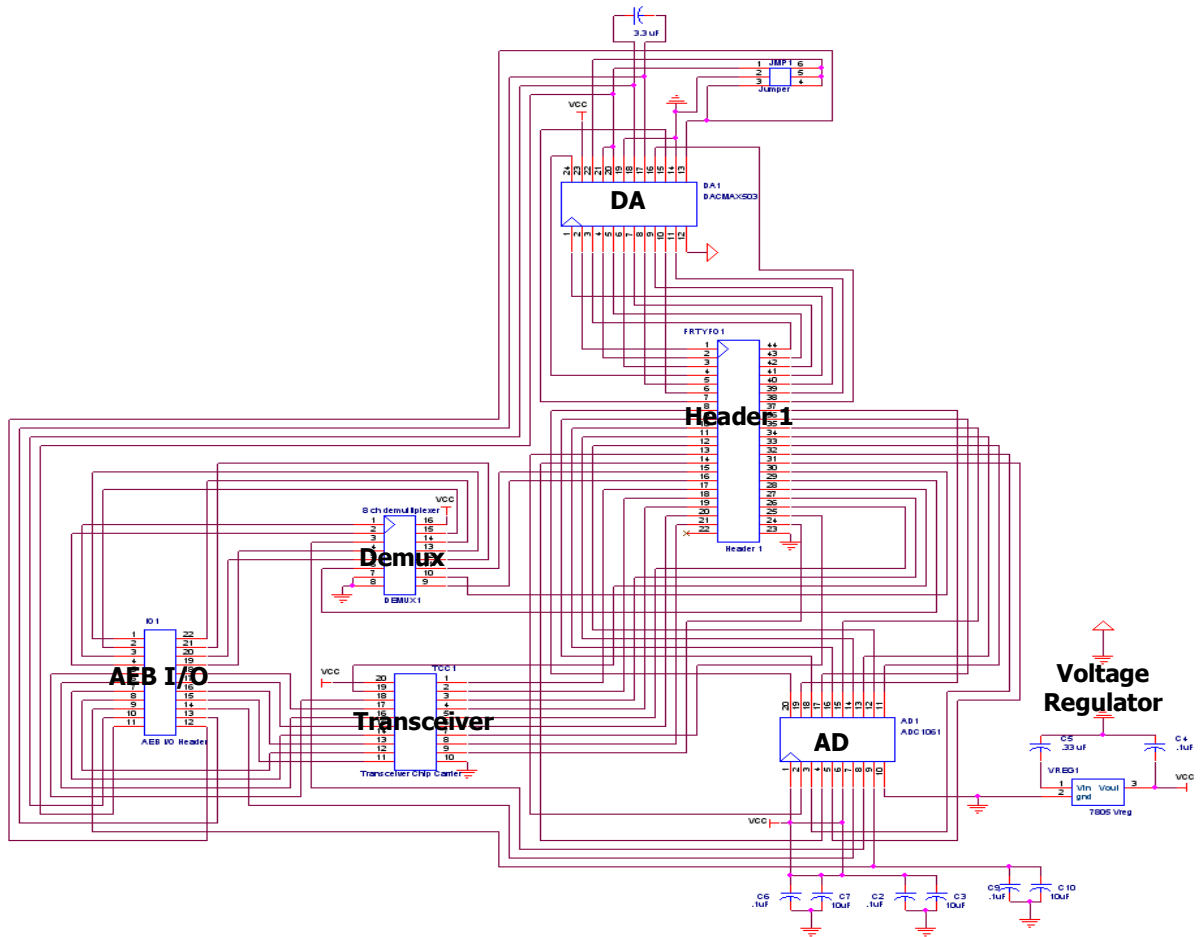


Figure 5. Header 1 Schematic

Figure 5 shows how Header 1 is interfaced to the D/A, A/D, and 8 bits of buffered inputs. Analog inputs are provided through the AEB I/O header and buffered with the transceiver. Eight signals are also fed to the demultiplexer which is interfaced to the A/D to give it eight channels of analog input instead of the one channel that the chip provides. The voltage regulator is also shown in figure 5, although it can be placed anywhere since all Vcc (+5V) and ground nodes are automatically tied together.

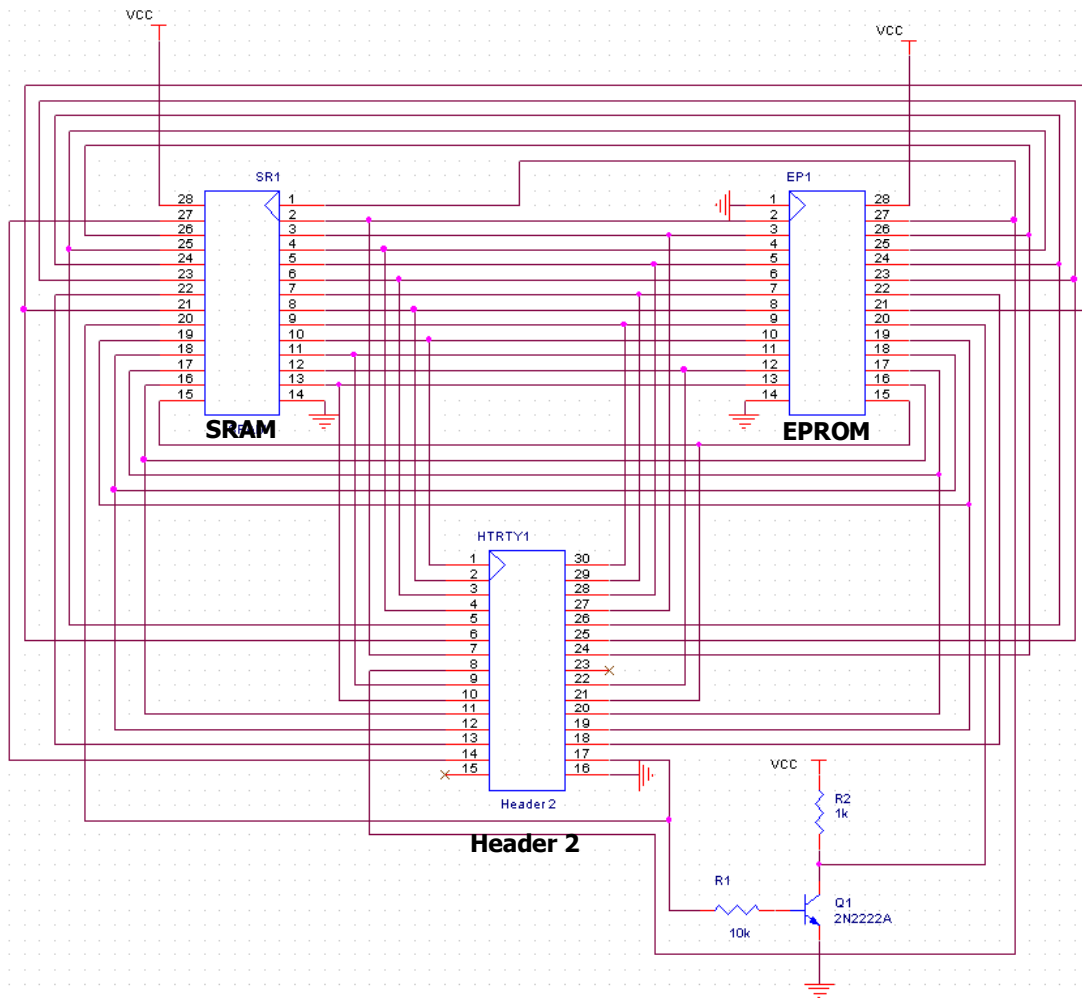


Figure 6. Header 2 Schematic

Figure 6 shows Header 2 interfaced to the EPROM and SRAM. To save space on the board, the address and data lines of both chips are tied together. As a result, it is necessary that only one chip can be on at a time. To ensure that this is the case, a BJT inverter is used to drive the chip select pins on each device which won't allow for both select lines to be active at the same time.

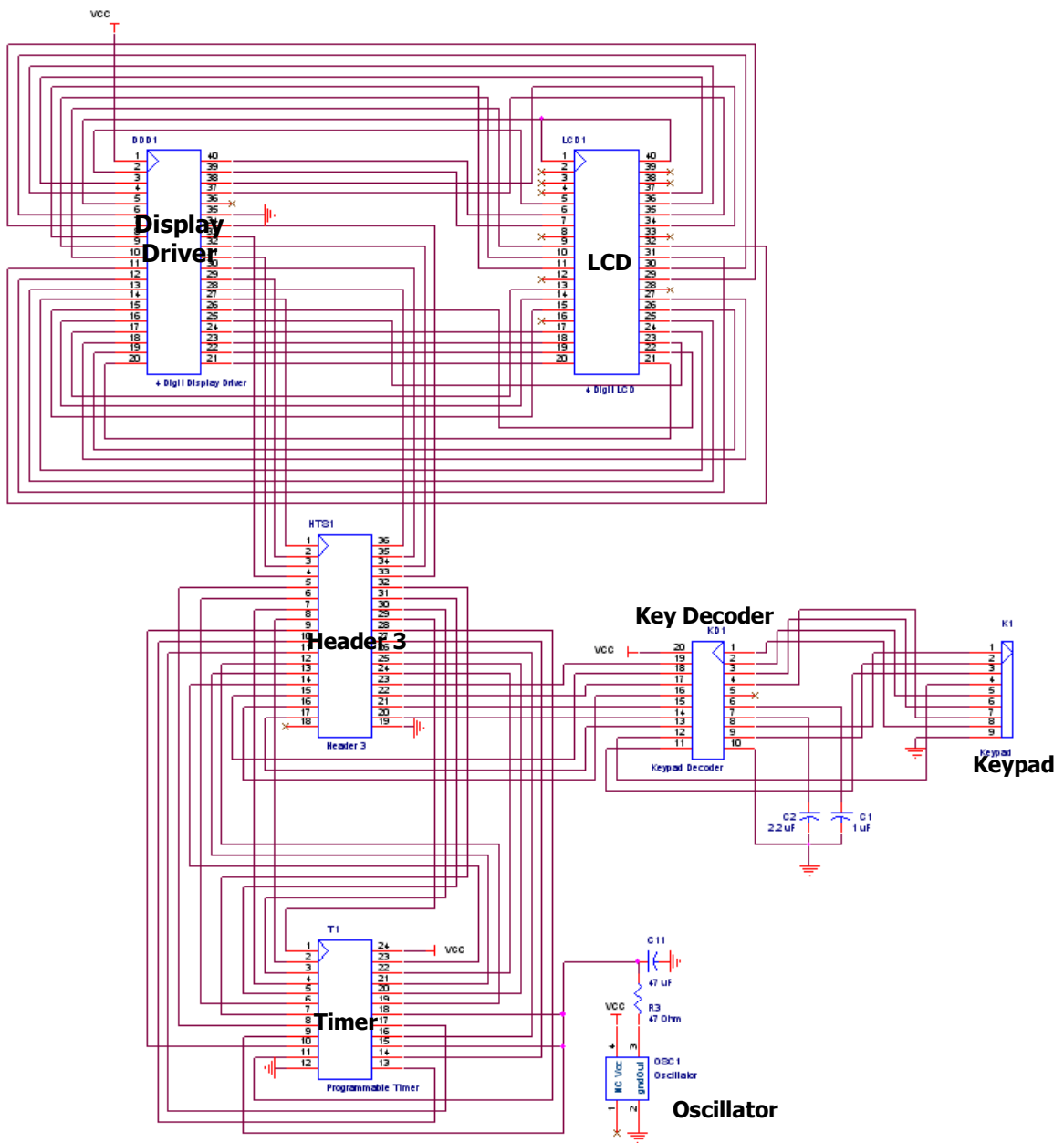


Figure 7. Header 3 Schematic

Header 3 provides the interface for the four digit LCD screen using a display driver, a 16 button keypad interfaced through a keypad-decoder, and a programmable timer which has clocked inputs from a crystal oscillator that is placed in a socket to allow the user to alter the frequency of the oscillator.

Once the entire schematic was created, a design rules check was done to ensure all connections were valid, and then a netlist was generated. The netlist is a technical listing of all nodal connections made in the schematic. When creating a new layout file (.MAX), the netlist is loaded and used to translate the schematic to a physical layout using the footprints that are associated with each component. All of the components are initially placed in an unorganized manner called the “rats nest.” First, a board border must be placed to define a region that components must be placed in. From there the parts were placed on the board based first on the necessity for a component to be in a particular location (e.g., such as the headers or DC input jack which need to be towards the edge for convenience of connection). The remaining parts were placed based on how interconnection between one another to reduce route length and minimize cross talk interference between the routes. The board layout is shown in Figure 8.

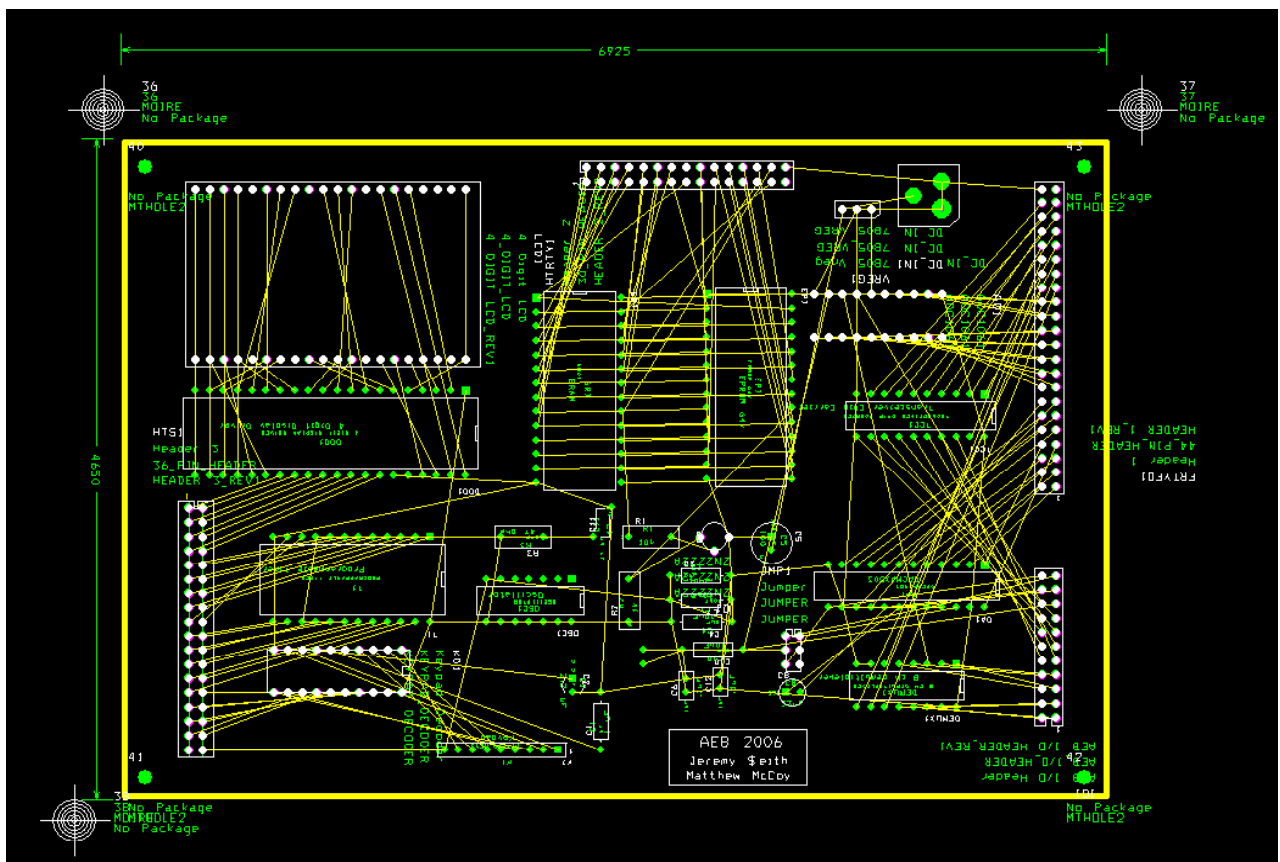


Figure 8. Board Layout

While there is a method to board layout, it is ultimately a skill that is developed with experience. However, OrCAD Layout provides a feature to allow the designer to visualize how well the board was laid out and how easy the routing process will be. Originally we arbitrarily chose a four layer board design. The connection density graph for this is shown in Figure 9.

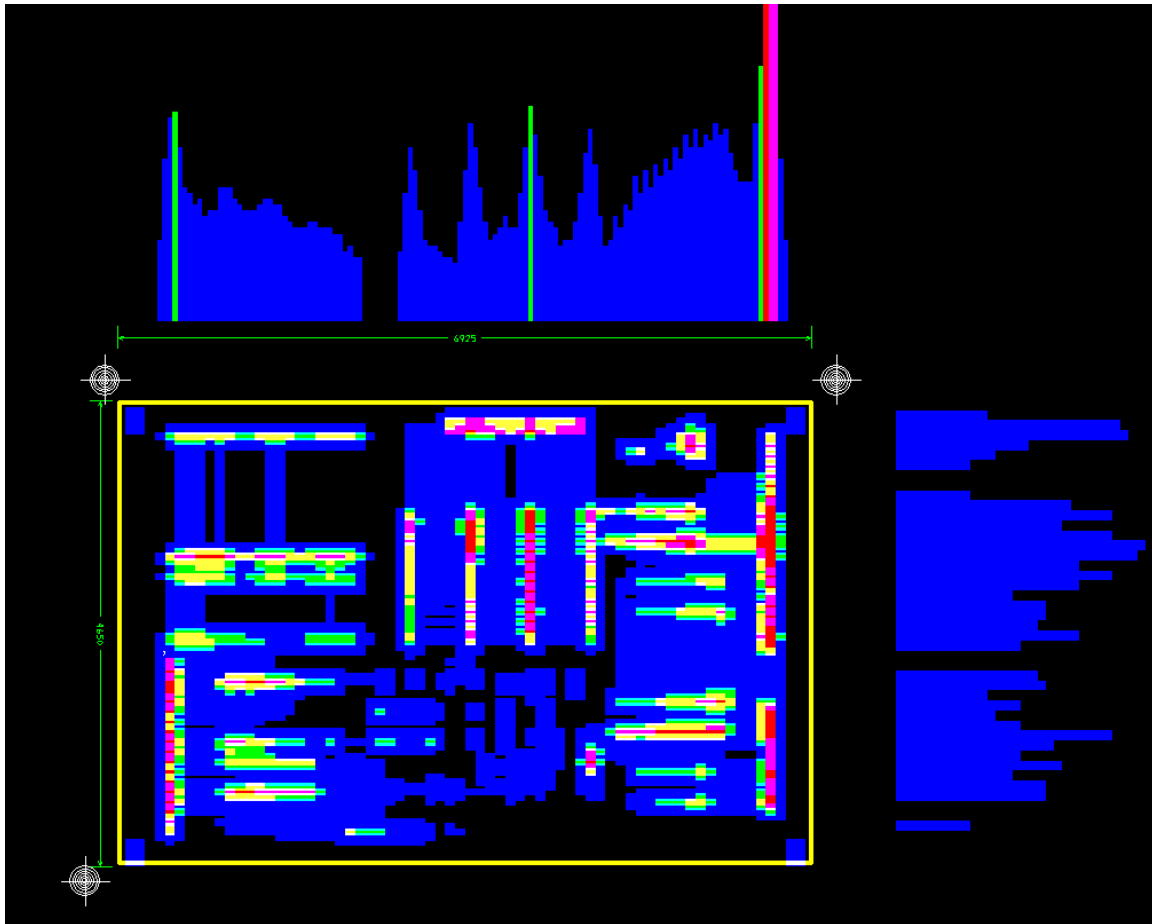


Figure 9. Four Layer Board Connection Density Graph

Red and purple indicate high connection density while blue represents low density. As a general rule of thumb, if more than 25% of the board is in high density problems routing the board are almost guaranteed. Once the board was at acceptable density range, it was routed using OrCAD Layout's autorouter. The result is shown Figure 10. The four layers are represented by each of the four route colors.

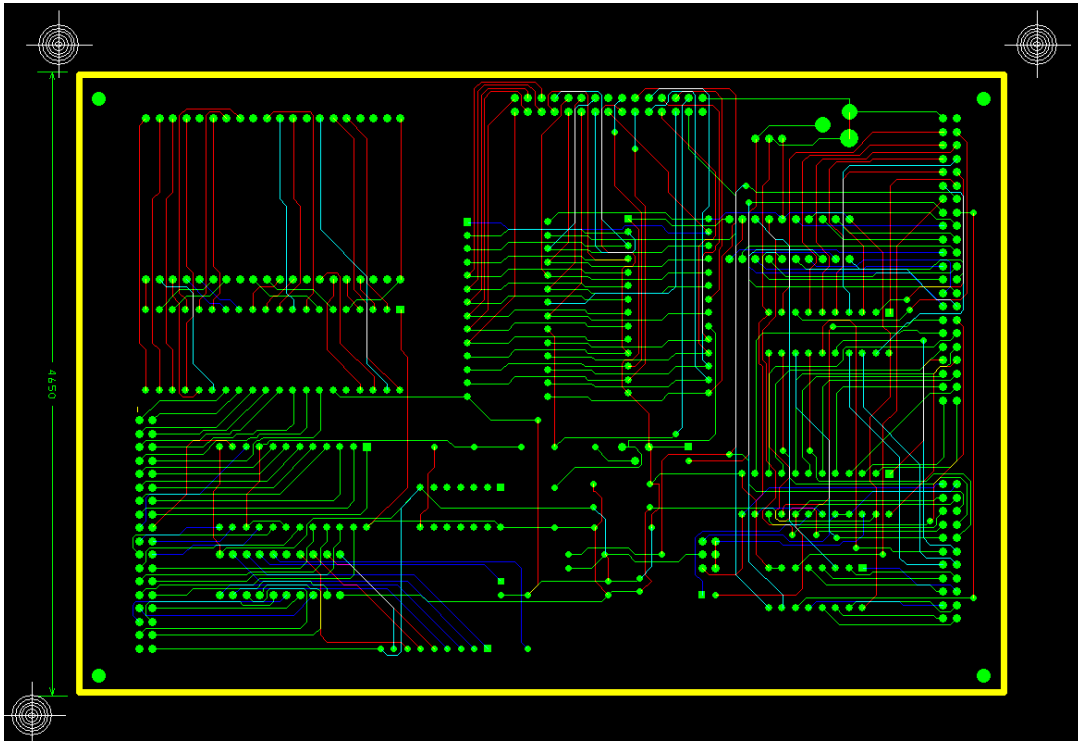


Figure 10. Four Layer Routed Board

After further research and discussion it was realized that costs difficulty of assembly and maintenance for boards of more than two layers increases dramatically. For these reasons a two layer board design was chosen. As a result the connection density increased as expected, but was still at an acceptable level as shown in Figure 11. The two layer routed board is shown in Figure 12.

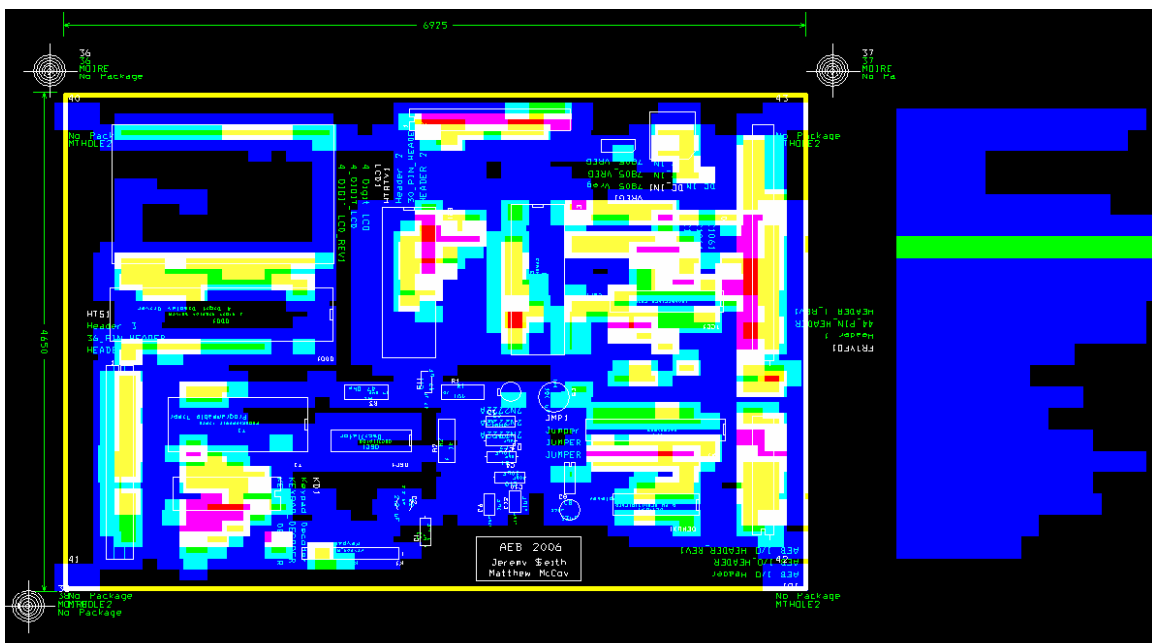


Figure 11. Two Layer Board Connection Density

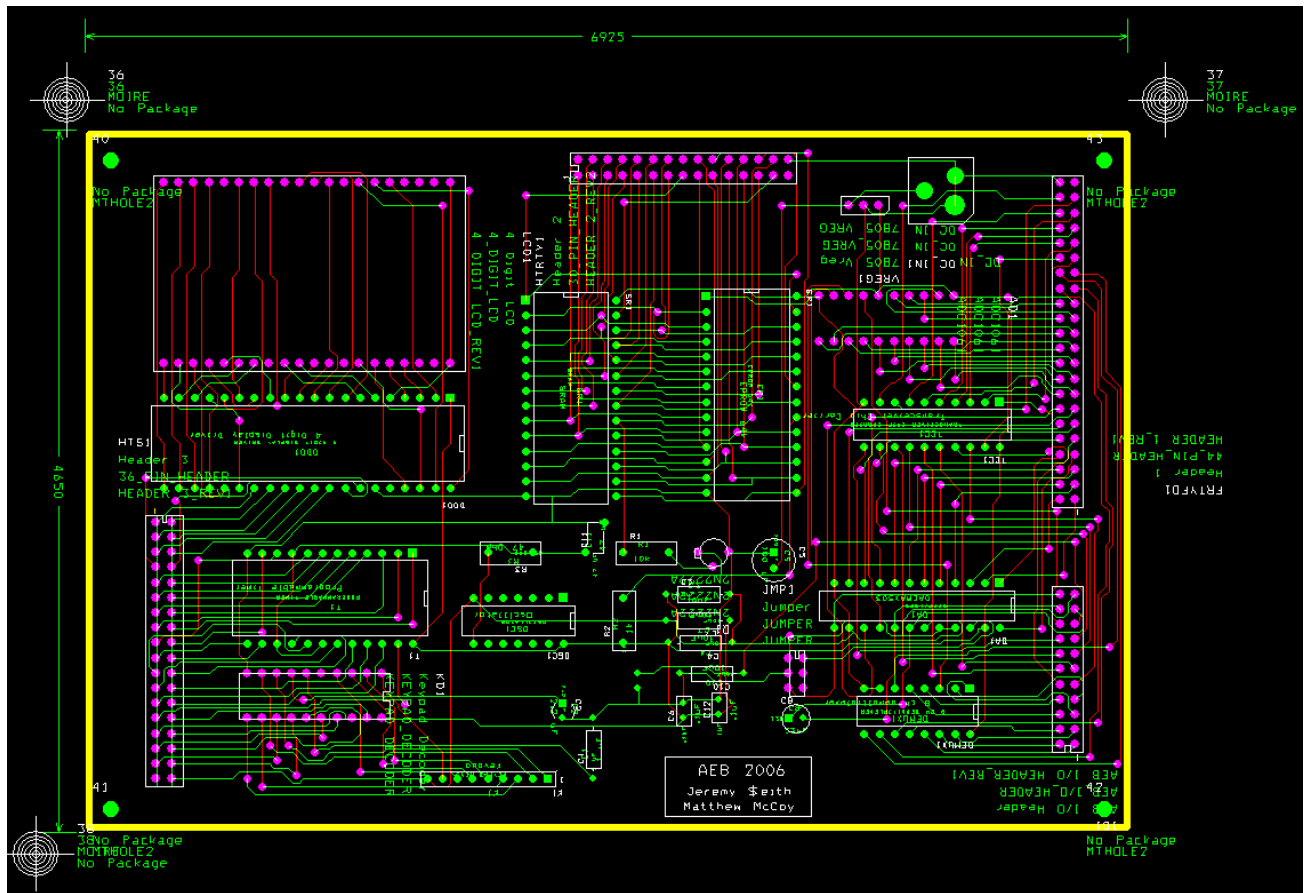


Figure 12. Two Layer Routed (Final) Board

The two layer board routed successfully and was the final design selected. With the layout and routing completed, board finalization was undertaken. This consisted of generating the silk screen, drill chart, and the gerber files. These files are for use specifically by the PCB manufacturer and for assembly of the board. The silk screen contains information such as labels, pin locations, chip orientation, and any other useful information that would be useful when looking at the board. A close up of the silk screen is shown in Figure 13. The drill chart can be seen in Figure 14. The gerber files are written in RS274X high level control language, and is an industry standard language which contains information that allows the photoplotter to very precisely draw out the board. This code is automatically generated by OrCAD Layout so it was not necessary to learn. An example of this code is shown in Figure 15.

Collecting those files is the final step before sending the design to the PCB manufacturer to have the board made. Although the board has yet to be fabricated, the board will resemble the board layout shown in Figure 16.

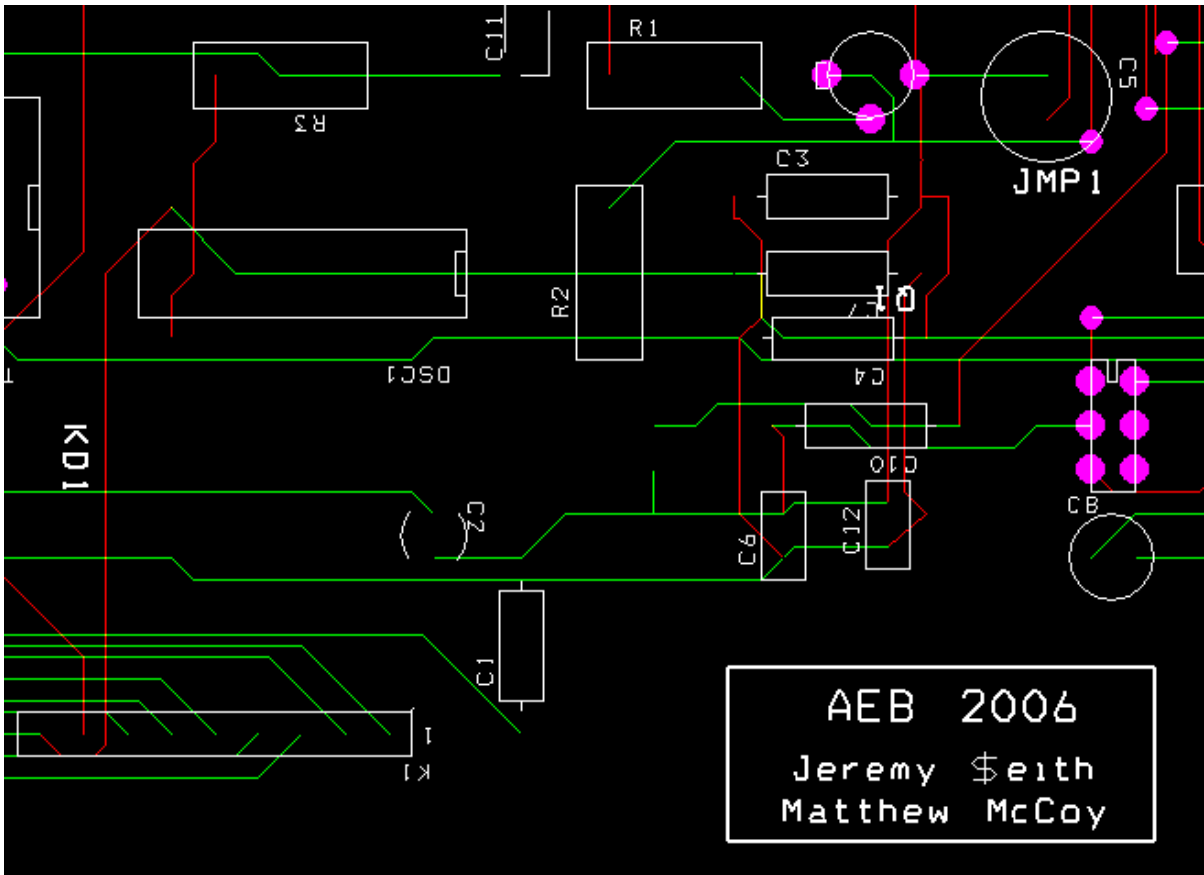
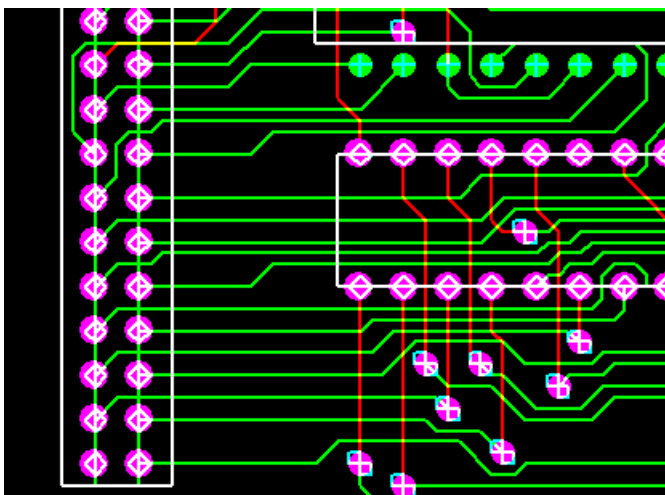


Figure 13. Silk Screen Layer



DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
⊠	0.028		101	
×	0.031		20	
+	0.034		213	
◇	0.038		224	
○	0.110		4	
⊠	0.120		2	
⊠	0.140		1	
TOTAL			565	

Figure 14. Drill Layer and Drill Chart

```

G04 G36/G37 Polygon Example ***
%MOIN*%
%FSLAX24Y24*%
%IPPOS*%

%ADD10C,,, *%           here we define some apertures
%ADD11C... *%
%ADD12C... *%
G04*
%LPD*%
G54D10*                 select D10
G01*
G36*                   switch into polygon mode. The diameter and
                        shape of D10 no longer matters.

X123Y123D02 *          move to initial position with pen up
X234D01*               draw a line (edge)
Y456D01*               draw a line (edge)
X234D01*               draw a line (edge)
Y123D01*               draw a line (edge) back to original start
G37*                   end polygon mode.

```

Figure 15. RS274X Sample Code

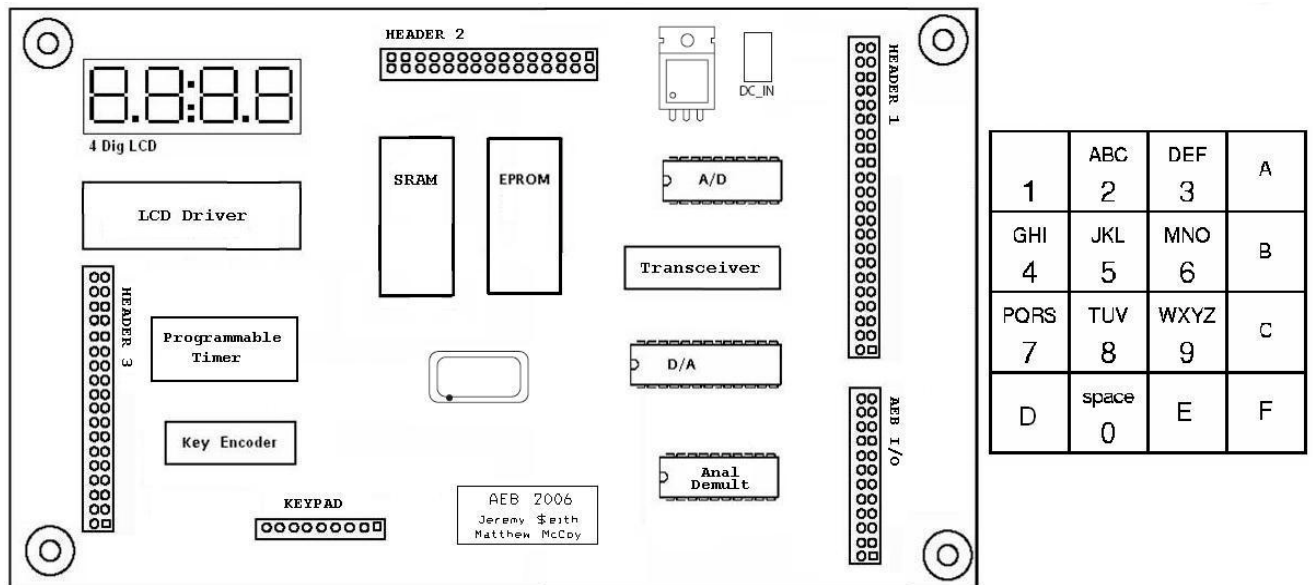


Figure 16. AEB Layout

RESULTS AND CONCLUSIONS

With the help of the Altera UP2 expansion board professors will be able to create labs that will involve a much more in depth digital design and students will be able to implement more complex designs in their projects while having the assurance that the AEB will protect components from possible error in connection.

Header Connection Chart

Header 1 pin #	DA	Header 3 pin #	LCD Driver
1-8	D(0-7)	1-4	B(0-3)
5,6	S0,S1	5-7	D(1-4)
7,8	D8,D9		Timer
9,10	A0,A1	9-16	D(0-7)
11	WR'	17	Out0
12	CS'	18	Gate0
13	CLR'	19	Out1
14	LDAC'	20	Gate1
	AD	21	Out2
15-24	DB(0-9)	22	Gate2
25	INT'	23	A0
26	S'/H	24	A1
27	RD'	25	CS'
28	CS'	26	RD'
	Demux	27	WR'
29-31	S(0-2)		Keypad Decoder
32	E'	28-32	A-E
	Transceiver	33	DAV
33	Dir	34	OE'
34	OE'	35	NC
35-42	B(0-7)	36	Gnd
43	NC		
44	Gnd		
		I/O Header pin #	Demux
		1-8	A(0-7)
			Transceiver 1
		9-16	B(0-7)
			AD
		17	Vref+
		18	Vref-
			DA
		19	RefOut
		20	RefGnd
		21	Vout
		22	VrefIn
Header 2 pin #	EPROM/SRAM		
1-15	A(0-14)		
16	NC		
17-24	Q:I/O(0..7)		
25	:OE'		
26	G':		
27	:WE'		
28	E':CS'		
29	NC		
30	Gnd		

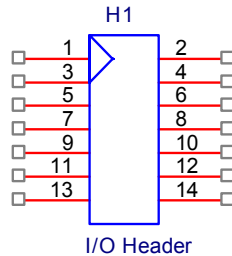


Figure 17. Header Numbering Scheme