PC Based Logic Analyzer

Complete System Level Block Diagram

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Introduction:
A logic analyzer is an instrument that displays digital signals. It functions much like an analog oscilloscope except it only displays four levels: low, high, tri-state and indeterminate; it also samples more lines. This project will create a PC based logic analyzer for use in Junior laboratory. It will have external conditioning hardware (known as a POD) connected to the PC. The PC will provide a Graphical User Interface (GUI), triggering, and signal display. This data flow is seen in Figure 1.

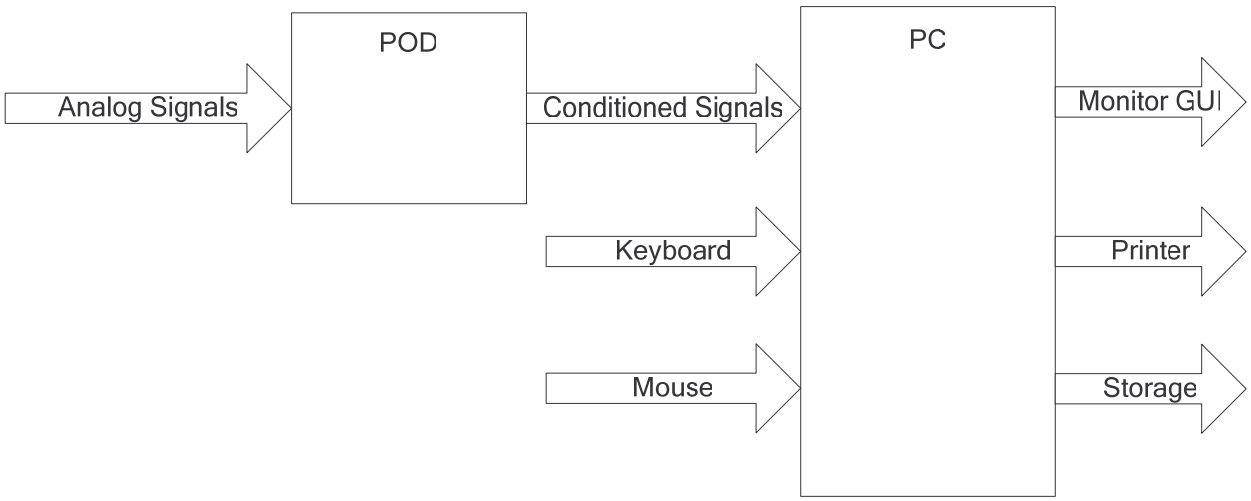

Figure 1: System Block Diagram

Inputs:

Analog Signals	Signals on the POD's probes. These can be TTL or CMOS based.
PC Commands	Commands entered using keyboard and mouse.

Outputs:

Monitor Display	Displays captured data, trigger signal, cursors and basic Windows functions (print, save etc.)
Printer	Prints the displayed waveform.
Storage	Saves waveform as an image

System Description

POD: This will accept analog signals on 8-16 data lines. The signals originate from TTL or CMOS based circuits. The POD will condition the signal to be transmitted to the PC via USB.

PC: The software will receive conditioned signals and display them in a user-friendly manner. It will provide several forms of triggering, cursors, zooming, etc. and standard window features.

Modes of Operation

Setup Mode: In this mode, the user selects the desired threshold levels for the analog signal type (TTL or CMOS), the number of lines to be sampled, the trigger condition, and the sampling method (synchronous or asynchronous).

Sample Mode: In this mode, started by the user, the analyzer collects the conditioned signals based on the selected triggering method.

Display Mode: This mode is entered automatically after the buffer is filled and the trigger occurs. The display can be zoomed and the cursors moved.

POD Functionality

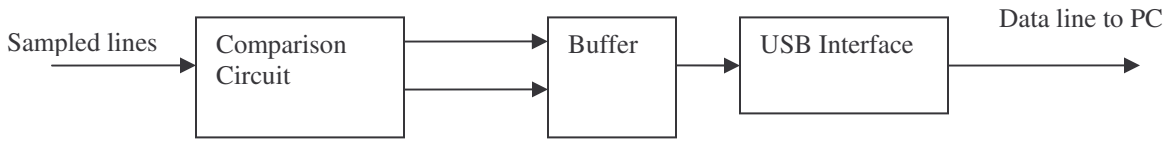

Figure 2: POD Block Diagram

Inputs:

Sixteen lines	These are the lines that are of interest to the user. They can be TTL or CMOS type. In addition, one of the signals may be designated as a clock signal on the target device and can be used for synchronous sampling.

Outputs:

Data line to PC	This is the sampled data in a 2-bit per sample per line form. A packet is sent on this line and USB protocols are used.

The POD is the sampling device for the logic analyzer. The POD has eight or sixteen digital lines configured to respond to a TTL and/or CMOS signal levels. It samples them synchronously using a designated clock line or asynchronously using an internal clock. For synchronous mode, the clock signal coming from the device under test (DUT) dictates when samples are taken, thus creating the appearance that all signals on all lines change on the clock. This is useful for simple testing; it allows the user to quickly see what happens in the device through each of its clock cycles. In asynchronous mode, all sixteen lines are sample lines. An internal clock set at a very high frequency dictates when samples will be taken. This is useful for allowing the user to see the independent activity of lines during a DUT's clock cycle. Moreover, this allows for much more detailed debugging. The comparison circuit determines one of four states for each line. The comparator can classify signals as high, low, intermediate signal (between high and low thresholds), or no signal (a High-Z condition). Once the state has been determined, the data is sent in the form of 2-bits into a buffer. Once several samples for all sixteen lines have been collected in the buffer, the buffer sends the data to the PC through the USB interface. More detail on the separate sections can be seen in figures below.

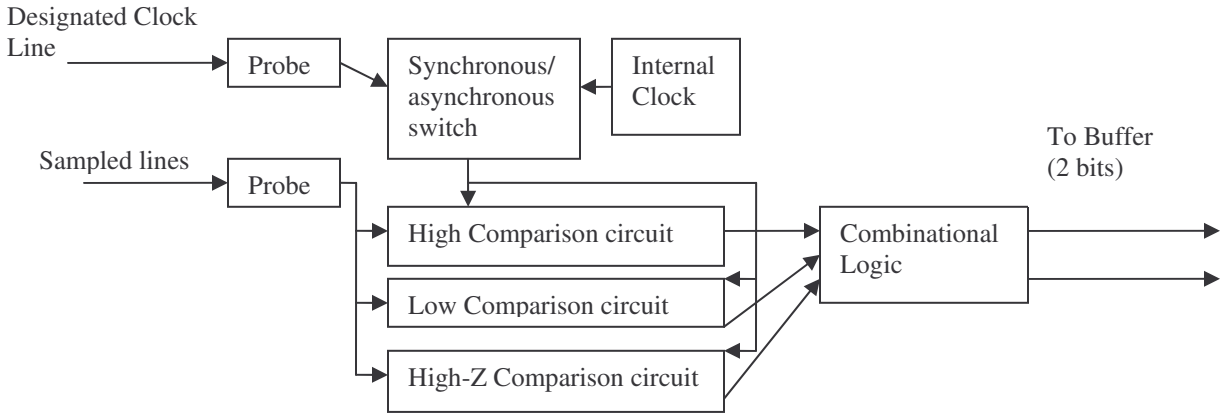

Figure 3: Comparison Circuit Block Diagram

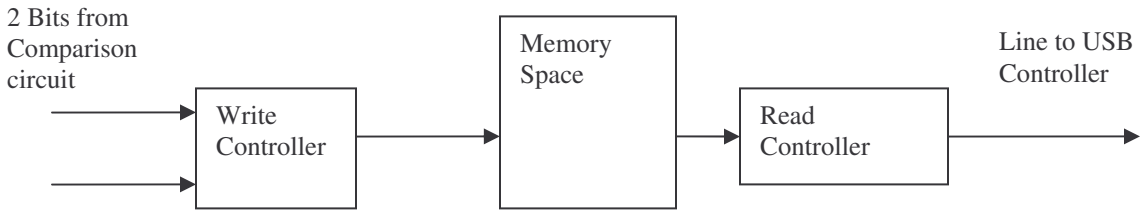

Figure 4: Buffer Block Diagram

Figure 5: USB Interface Block Diagram

PC Functionality

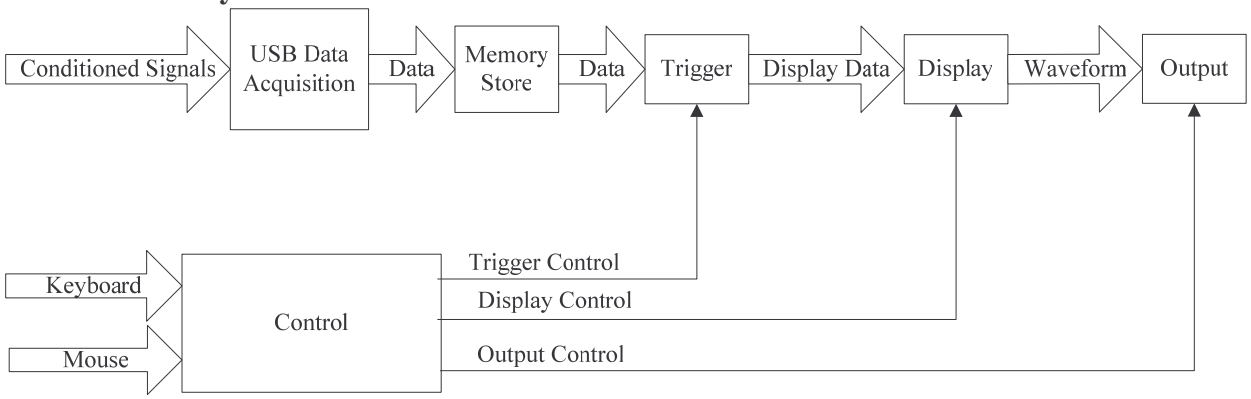

Figure 6: PC Block Diagram

PC Inputs:

Conditioned Signals	Signals sent from the POD to the PC with all sampled data in packet form using USB protocols.
Keyboard/Mouse	Commands entered using keyboard and mouse to setup trigger conditions, change display format, save the waveform, setup, and hardcopies.

Outputs:

Monitor Display	Displays captured data, trigger signal, cursors and basic Windows functions (print, save etc.)
Printer	Prints the displayed waveform.
Storage	Saves waveform as an image

The PC is the user interface to the logic analyzer. The conditioned signals are received by the PC and the raw data is extracted from the USB packets. The raw data is then stored in memory. A significant amount of data will be kept in memory such that all trigger conditions could be adequately displayed based on the samples contained in memory. The user can set the trigger conditions using the keyboard, the mouse and the GUI. When the trigger condition is met, the software will display the samples that are relevant to the time at which the trigger condition was met. The software will also display a user-controlled-length of data both before and after the trigger condition. This allows the user to see data prior to the trigger point, to see data after the trigger, or see a percentage of data before and after the trigger point. The displayed image is going to be based on the user's choice of sample rate. If a slower sample rate is chosen, then the user will be able to see a longer length of time in around each trigger but with less resolution; if a faster rate is chosen, more detail is shown, but the length of time displayed around a trigger is less. More detail in each section of the block diagram can be seen in the Figure 7 and Figure 8.

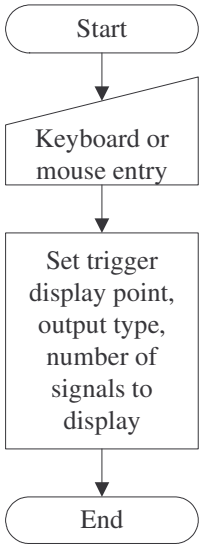

Figure 7: Control Block Diagram

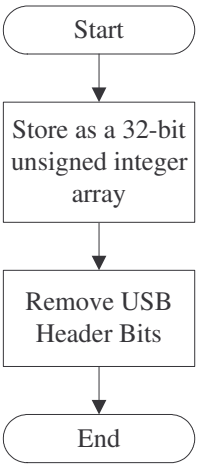

Figure 8: USB Data Acquisition

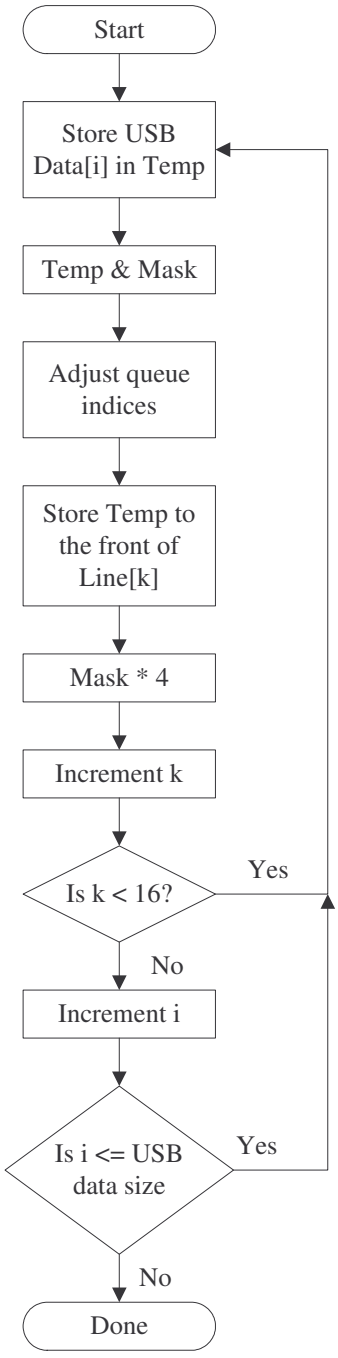

Figure 9: Memory Store

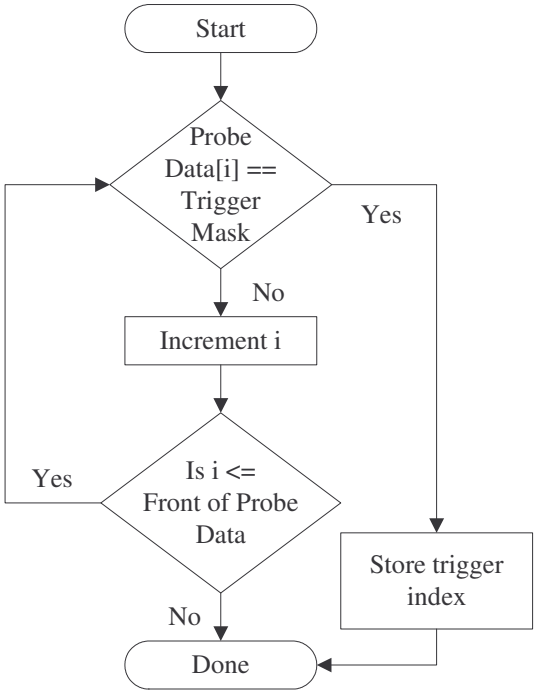

Figure 10: Trigger Block

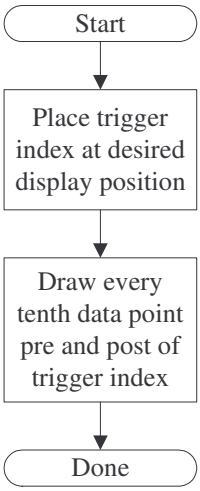

Figure 11: Display Block

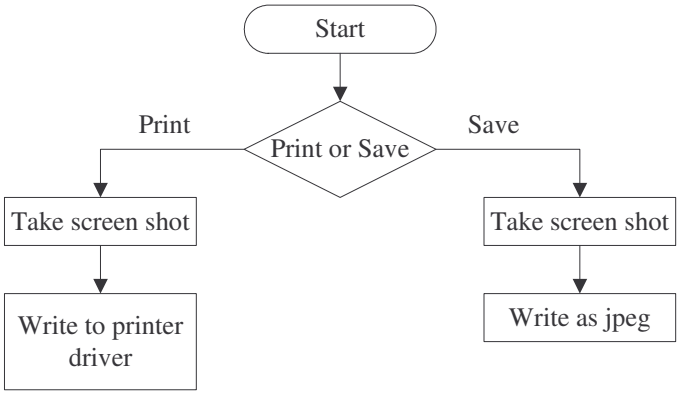

Figure 12: Output Block