

To: Dr. Vinod Prasad
 Dr. Thomas Stewart

From: Jeremy Barsten – ibarsten@hotmail.com
 Jeremy Stockwell – screwbal@bradley.edu

Re: Senior Capstone Project

Subject: Functional Description

The objective of this project will be to implement an all-purpose digital-signal processor utilizing FPGA's, that can be used in a variety of applications. These can range from cellular and control applications to various types of audio and video processing. The purpose of this processor would be to manipulate signals according to the specific application so that the overall efficiency of the application is improved. Below is a basic block diagram of this project showing the inputs and outputs of this project.

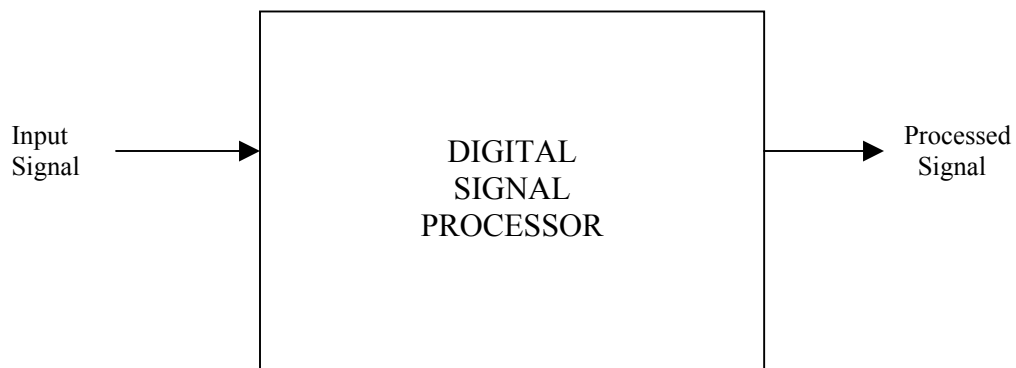


Figure 1: Overall block diagram of the digital signal processor.

Digital Signal Processing is the process of manipulating a digital input utilizing multipliers and adders. We plan to implement a second order Direct Form II realization of an IIR filter.

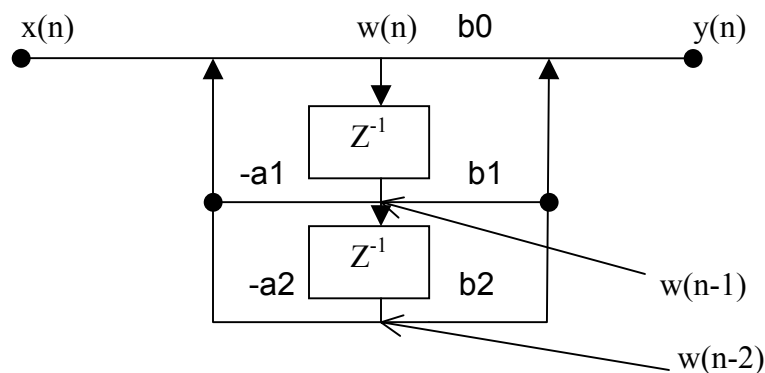


Figure 2: Direct Form II realization of IIR Filter

Utilizing this format we can derive the equations necessary to process the signal.

$$y(n)=b_0*w(n) + b_1*w(n-1) + b_2*w(n-2), \text{ where } w(n)=x(n) - a_1*w(n-1) - a_2*w(n-2)$$

This simplifies to:

$$Y(n)=b_0*x(n) + b_1*x(n-1) + b_2*x(n-2) - a_1*y(n-1) - a_2*y(n-2)$$

The processor can be used for a infinite amount of applications by simply adapting the coefficients $b_0, b_1 \dots$ etc for each specific application. The following stages will be a part of the processing system: 16-bit analog-to-digital converter, 16-bit multiplier, 32-bit adder, memory management, and a 10 or 12-bit digital-to-analog converter. The following stages will be briefly discussed in the next sections.

Signal Converters

Even though some digital signals are sent and received globally, many of the signals today are sent and received in analog form. For this reason, two converters must be included in the design of this digital processor. A 16-bit analog to digital converter will be used to convert the incoming signal to a digital one. This particular A/D converter will be used because they are readily available. However, once the processing has taken place, the resultant digital signal will be thirty-two bits wide. The design will account for this by implementing some form of truncation so that the least significant bits are discarded from the output signal. The amount of truncation will be determined later based on experimentation.

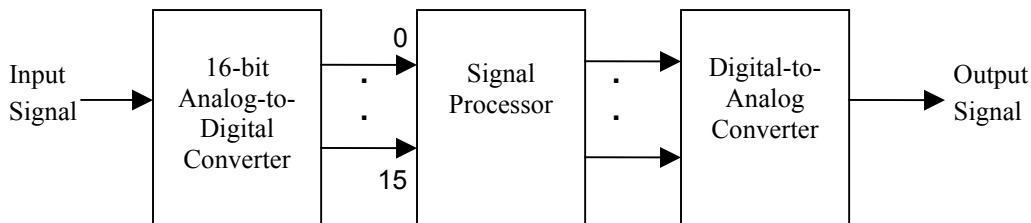


Figure 3: Block diagram showing signal converters' connection.

Adder, Multiplier, and Storage

The basic structure of any signal processor consists of an adder and multiplier used to process the signal. A 16-bit by 16-bit multiplication will take place and the resultant 32-bit answer will be fed into the adder circuit. This will then adjust the value of the signal based on the previous value that was stored in memory. The 32-bit signal will be truncated after exiting the adder to reduce the data to a more manageable size. We will investigate architecture of high speed arithmetic circuits for improved speed. Also note that the data being manipulated consists of both positive and negative values. Therefore, all processing will be done in two's complement.

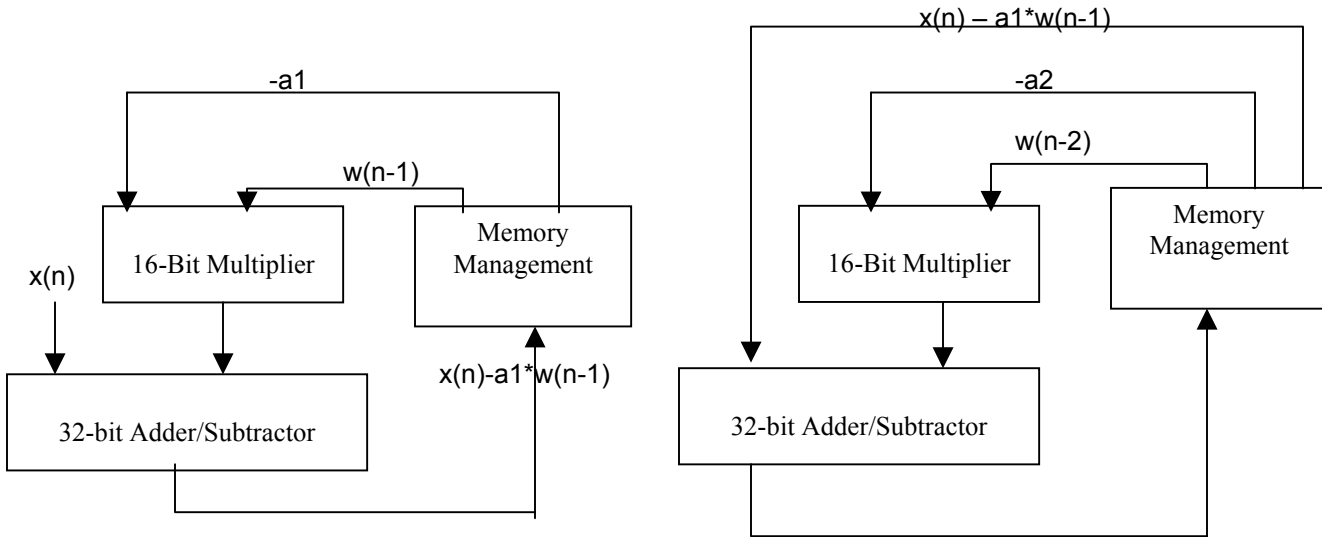


Figure 4: Block diagram showing consecutive steps in the data management.

Memory Management

Figure 4 shows a sample for two consecutive cycles of the data management. The truncated values from the adder and the coefficients that need to be multiplied for the specific application must be stored in the memory and be readily available for use. Not only is the memory management used for storage, but also is needed to control the data by delivering it to the appropriate device at the appropriate time.