To: Dr. Vinod Prasad
Dr. Thomas Stewart

From: Jeremy Barsten – jbarsten@hotmail.com
Jeremy Stockwell – screwball@bradley.edu

Re: Senior Capstone Project

Subject: Complete Block Diagram

This project will utilize FPGA and VLSI technology to construct a general digital signal processor. For this, a top-down design approach is implemented when dealing with each individual aspect of the processor. A general high-level block diagram of the device is shown in Figure 1. For this processor, there is only a single input and a single output for the entire system. A general signal will be

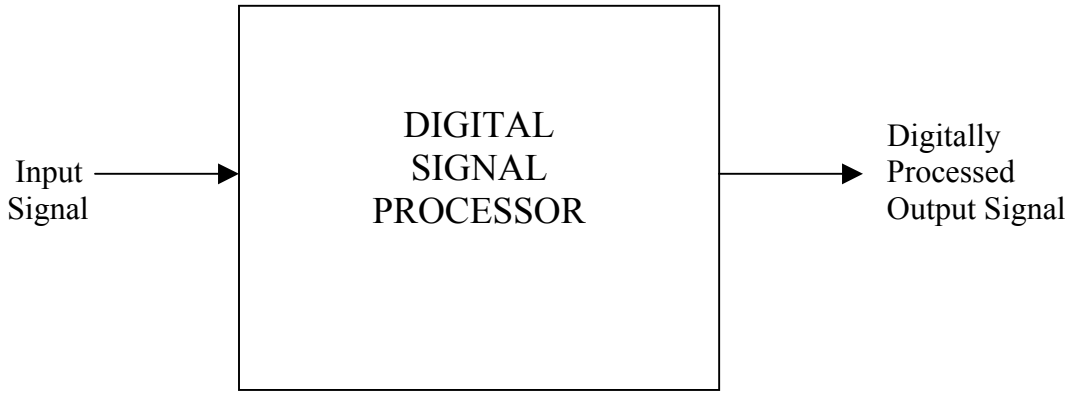

Figure 1: High-level block diagram of the digital signal processor.

sent to the system where it is digitally filtered and processed according to the individual application. In this project, the speed of the device is the main concern, not the signal. The system then produces a digitally processed signal that can be used by other devices.

The first stage of the processor is an analog-to-digital converter. The incoming signal must be converted to a digital one before it can enter the processor stage of the system. Because of their availability and cost, a 16-bit converter is used as the first block of our system. The resultant digital bits are then sent to the processor as shown in Figure 2 (on the next page).

The digital signal is then sent through a generalized filter. There are two inputs to this block of the system. The first input is the filter coefficients. These numbers are predefined and already programmed into the processor. By selecting the correct coefficients, the filter type and order can be determined. The second input to this block is the digital signal from the converter. Different applications will have different frequencies at which data will enter the system,

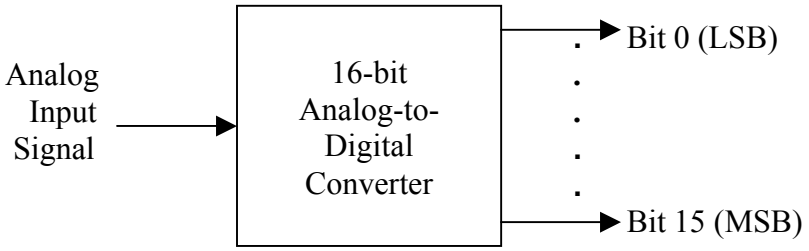

Figure 2: Block diagram of the analog-to-digital Converter.

and this filter chooses the correct frequency for the correct application. The output of the signal will be a digitally filtered signal that will be sent on to the next block of the system. The block of this filter is shown in Figure 3.

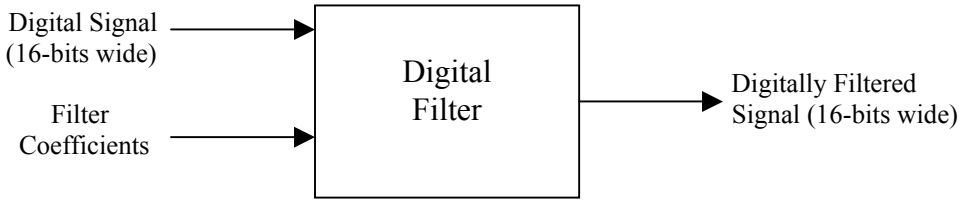

Figure 3: Block diagram of the general digital filter.

The next block in the system is the adder and multiplier circuits. Here, current signals are multiplied by internal coefficients (which have yet to be determined) and sent to the adder. The now 32-bit wide signal is added to previously stored signals. These previous signals come from a memory management block that will be discussed later. The block of the adder and multiplier circuit is shown in Figure 4.

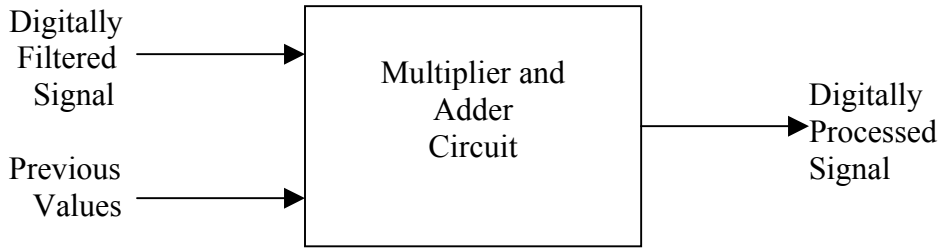

Figure 4: Block diagram of the multiplier and adder Circuit.

Another block that accompanies the adder and multiplier circuits is a memory management circuit. This block stores previously processed signals that have been truncated. Truncating the values before storing them and feeding them back to the adder circuit helps prevent overflow and keeps the bit-width of the signal stable. Otherwise, the number of bits would increase beyond 32 bits as signals are continuously passed though the processor. Therefore, a truncating

circuit is implemented before sending out a processed signal and storing the value for future calculations. These two blocks are shown in Figure 5.

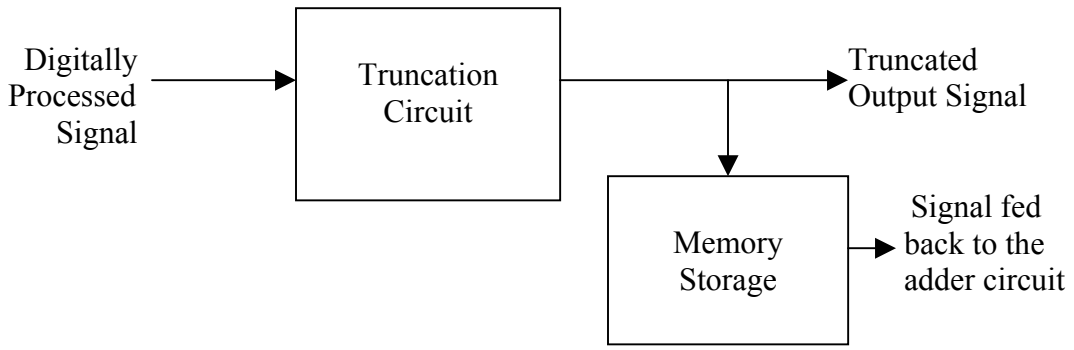

Figure 5: Block diagram of the truncation circuit and memory storage circuitry.

The final block in the system is a digital to analog converter. The signal is received as an analog one, and it needs to be output in the same way. However, the output signal has been truncated from its original 16 bits. At this time, the number of bits in the output signal has yet to be determined. This decision will be made later as we progress. The final block consists of a digital-to-analog converter that will produce the final analog signal. This block is shown in Figure 6.

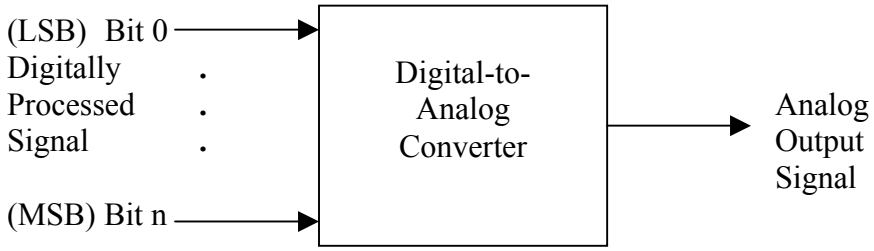

Figure 6: Block diagram of the digital-to-analog converter.