

# Design of a Memory Chip with Error Detection and Correction Codes

A (7,4) code, which is a 7-bit code word with a 4-bit information code, will be stored in a register. This information will be processed through error detection circuitry to determine if the transmitted data is correct. If the information needs to be corrected, error correction circuitry will correct the code and the new information code will be stored in a 4x16 memory chip. (Refer to Figure 1)

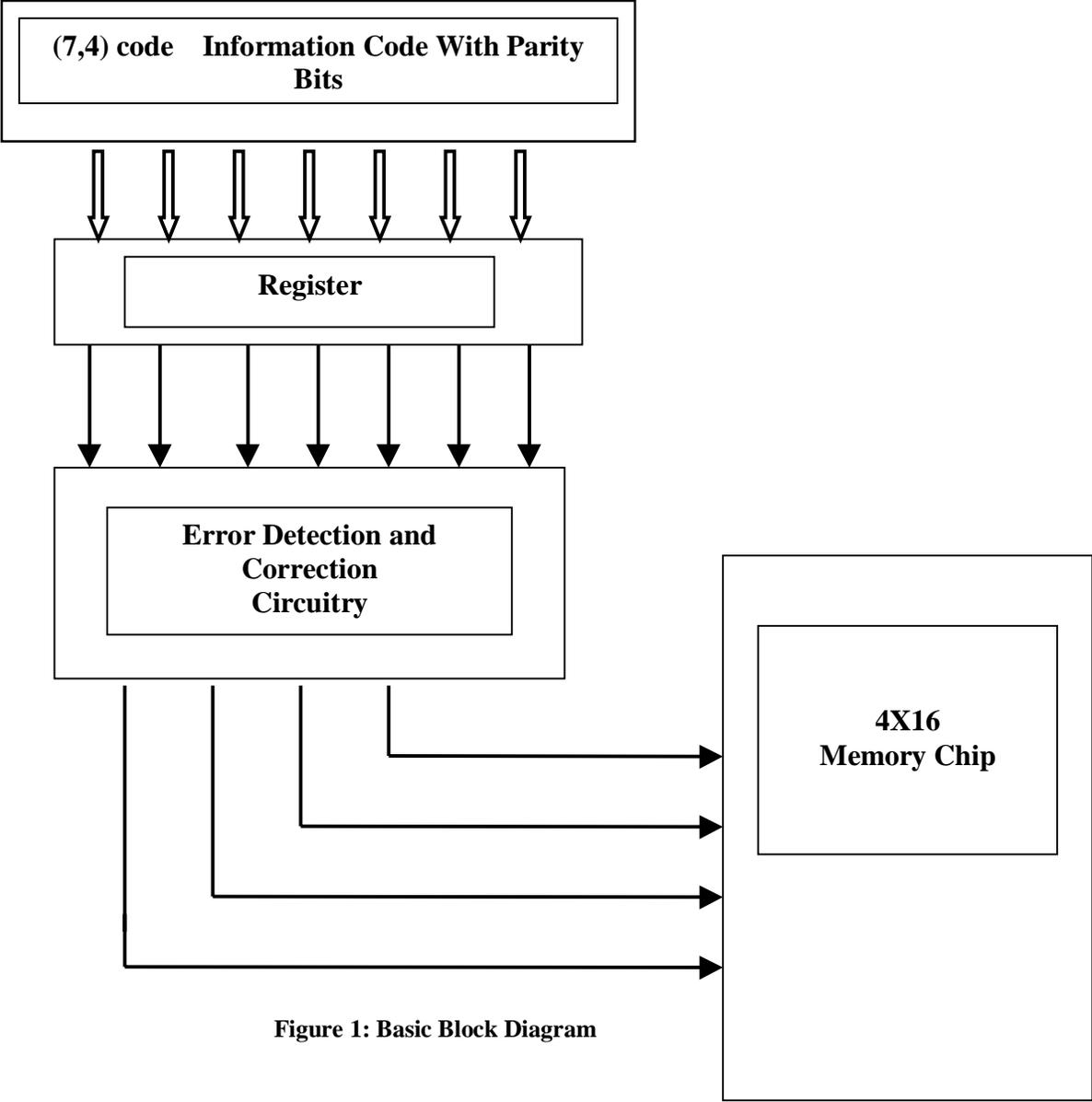


Figure 1: Basic Block Diagram

The definition of an error detection code is one which possesses the property that the occurrence of any single error transforms a valid code word into an invalid code word. This is done with parity bits. For this (7,4) code, three parity bits will be used, which is concluded from the 7 bit code word minus 4 bits of information ( $7-4=3$  parity bits). A code is error correcting if the correct code word can always be deduced from the erroneous word.

The distance,  $d$ , between two code words is the number of digits that must change in one word so that the other word results. To make an error detection code, the distance has to be 2 or greater. An error correction code with a distance, ' $d$ ', can correct ' $t$ ' errors if the minimum distance between 2 consecutive words is  $(2t + 1)$  or more.

The minimum distance for error detection is 2 or more, and for error correction, the minimum distance is 3 or more. For example, if the minimum distance is 3, the code can detect double errors and correct a single error.

Once an error has been detected, the circuitry will basically have to compliment the erroneous digit. This new information code will be ready for memory storage.

Every component in the block diagram will be designed and built in VLSI. The register which stores the code, the logic gates used for error detection and correction circuitry, and the 4X16 memory chip will be carefully implemented in VLSI and the IC chip will then be simulated through hardware. The project is still in the research and developmental stages.