FPGA Implementation of a PID Controller with DC Motor Application

Members	Advisors
Paul Leisher	Dr. Stewart
Christopher Meyers	Dr. Dempsey

This project aims to implement a digital PID controller by means of an FPGA. This system will be used to control a DC motor (driven by a PWM signal) which has a high degree of non-linearity and serves to test the performance of the controller. Our preliminary research has primarily focused on simulating the entire system, although recently we have begun work on the VHDL code to program the FPGA. Upon completion of the VHDL, we will begin testing and improving the overall system.

Outline

- Functional Description
- Division of Labor
- Matlab and Simulink Work
- Hardware Interfacing
- VHDL Work
- Achievements and Complications
- Closing

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Functional Description

This project will implement a digital "Proportional-Integral-Derivative" (or PID) controller in an existing DC motor system. The DC motor system will be controlled by a PWM signal. The system will be implemented in 'closed' loop form, which will correct the non-linearity and unreliability of the change in loads on the DC motor.

The entire system will be programmed in VHDL, and implemented on a FPGA Development Board. This will allow the user to input a desired RPM and be able to monitor the speed of the DC motor. It will also provide an economical solution to DC motor control.

System Inputs and Outputs

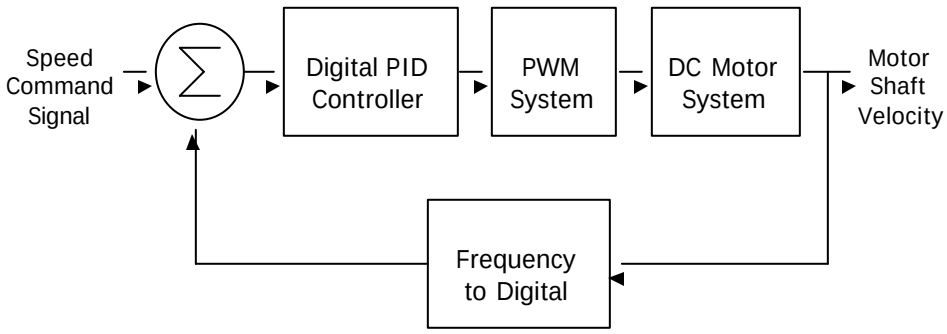
Inputs

- Speed Command Signal

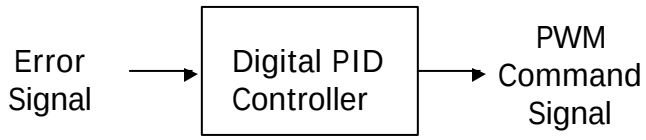
Outputs

- Motor Shaft Velocity
- System Display

System Block Diagram

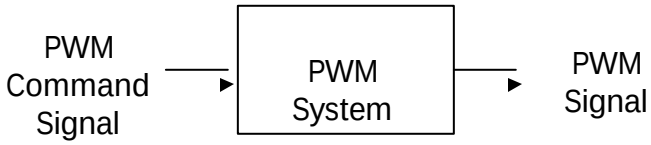


Digital PID Controller



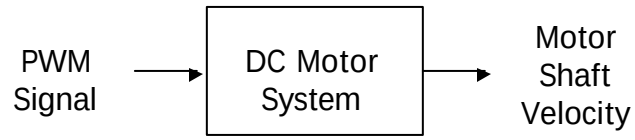
•Error Signal combination of desired input and motor shaft velocity
•PWM Command Signal computed based on Error signal to ensure linearity

PWM System



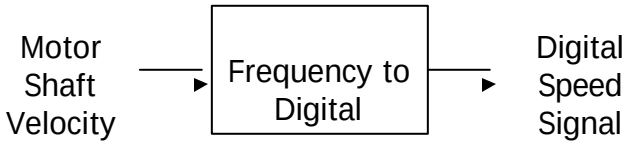
•PWM Command Signal used to create desired percent duty cycled signal

DC Motor System



•PWM Signal used with hardware to control DC Motor System
•Motor Shaft Velocity produced by encoder

Frequency to Digital Converter



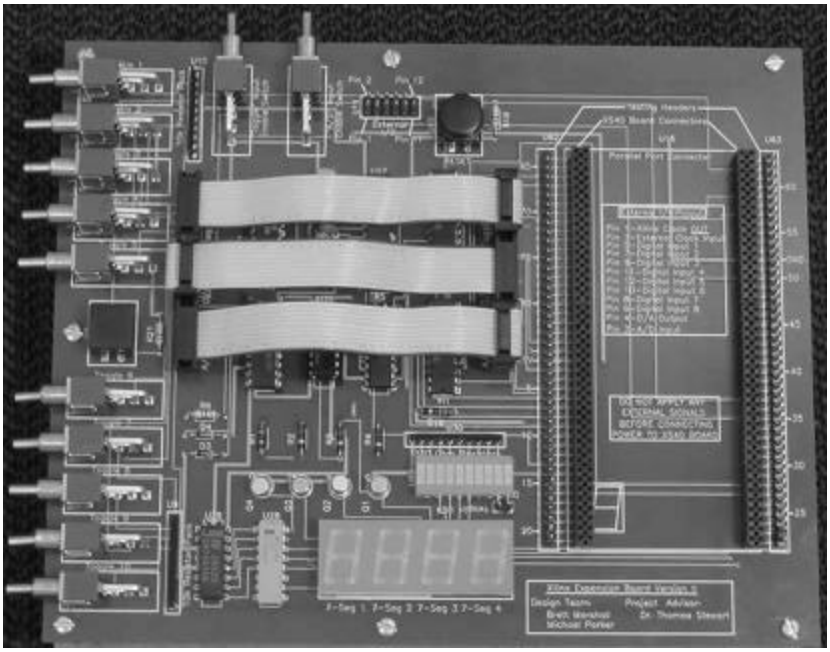
•Motor Shaft Velocity sent from encoder on DC motor
•Digital Speed Signal is a digital representation of motor shaft velocity

Modes of Operation

- Full Speed
- Off
- 0 to 860 RPM via user

FPGA Development Board

- Brett Marshall – 2000/2001 Senior Project



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Division of Labor

• Due to highly theoretical nature of project, most parts will be completed together.

Paul Leisher

- VHDL Framework
- VHDL Display and Encoder
- PID Controller

Christopher Meyers

- VHDL PWM Subsystem
- Hardware Interfacing
- PID Controller

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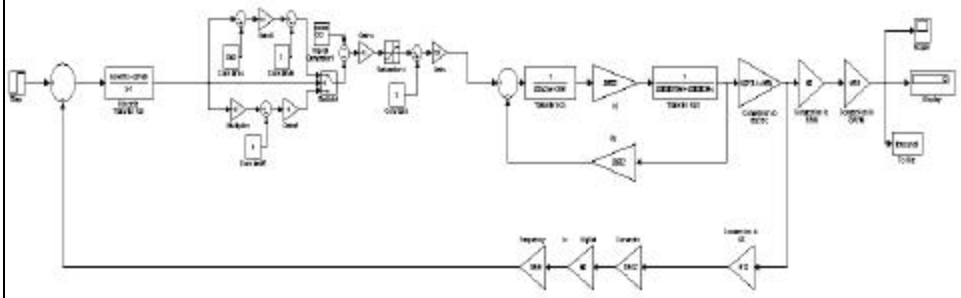
Matlab Design Program

- Shows uncompensated system plots
- Shows compensated system plots
- Determine Digital PID Controller coefficients

Simulink System Model



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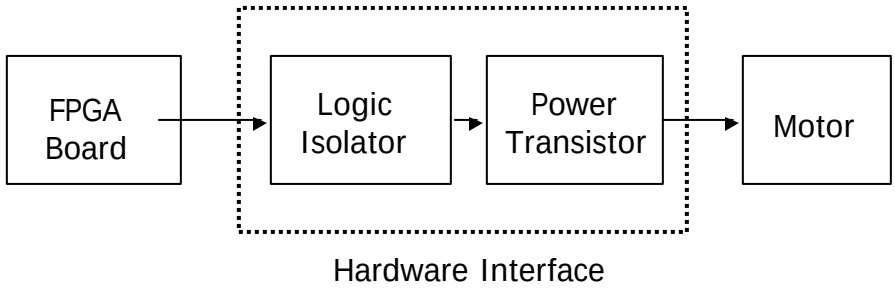
Hardware Interface

- Hardware was needed to
  - Interface FPGA to motor
  - Protect FPGA Development Board

Hardware Block Diagram



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VHDL Work

- PWM System
- Encoder to 7-bit number
- PID System
- Display System
- Error Signal & Command Input System

VHDL Work

- **PWM System**
- Encoder to 7-bit number
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PWM System

- Receives a number from the PID controller between 0-128 (7-bits)
- Uses internal counters along with the clock input to determine the PWM signal, by number comparison
- Includes out of range checks

PWM System

INPUTS

- 7-BIT Unsigned Number
- Clock
- Negative Trigger

OUTPUTS

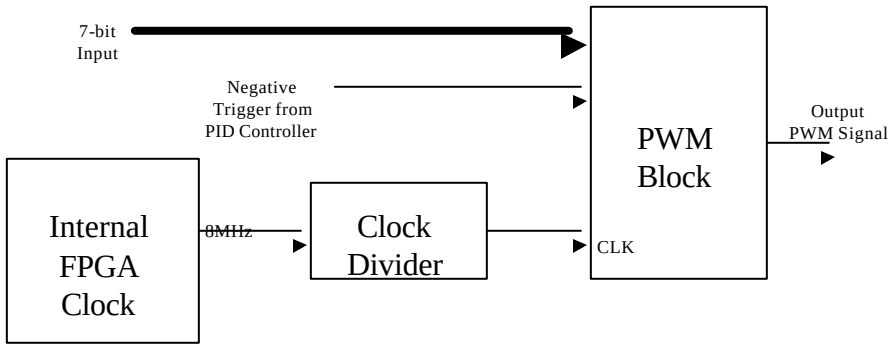
- Pulse Width Modulated Signal

PWM System

Problems

- Usage of an External Clock
  - Solution
    - Designed a VHDL block to divide an internal clock signal

PWM System Schematic



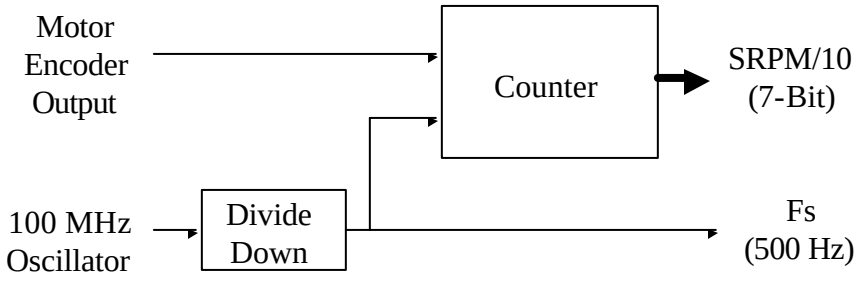
VHDL Work

- PWM System
- **Encoder to 7-bit number**
- PID System
- Display System
- Error Signal & Command Input System

Encoder to 7-Bit Number System

- This system converts the rotary encoder output of the motor (512 pulses per revolution) to a 7 bit number (0 to 86) where that number is one-tenth the speed of the motor shaft in RPM.
- Because the system sampling frequency is 500 Hz, this system is not fully accurate.

Encoder to 7-Bit Number System



Encoder to 7-Bit Number System

- This system works by counting the number of pulses that occur within T=2ms (fs=500Hz).
- This system is not performing well enough for our application.
- This system will be redesigned to measure pulse duration rather than to count pulses.
- This redesign will improve resolution, and hopefully, system performance.

VHDL Work

- PWM System
- Encoder to 7-bit number
- **PID System**
- Display System
- Error Signal & Command Input System

PID System

- First tried proportional control only
  - Results were “ok”
  - Results did not correlate very well to Simulink results, however, the general property of increasing proportional gain decreases steady-state error was observed
- Tried very basic PI controller
  - Results were horrible
- Work on PID system halted until Encoder-to-RPM block is redesigned.

VHDL Work

- PWM System
- Encoder to 7-bit number
- PID System
- **Display System**
- Error Signal & Command Input System

Display System

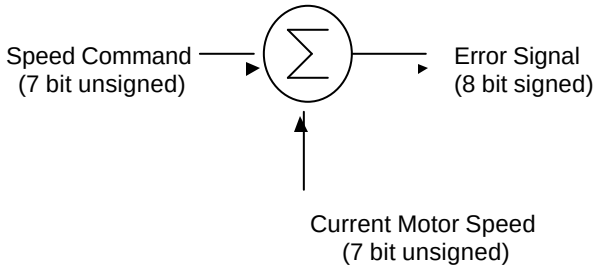
- This system allows for the display of either the current command input signal or the current motor speed (both in RPM).
- The user can switch between either display by means of an onboard toggle.
- This system utilizes three of the four onboard seven-segment displays.
- This system was rewritten so LED refresh rate is fast, but RPM displayed is ~1 sec. (This serves to allow the user to read the display more easily).

VHDL Work

- PWM System
- Encoder to 7-bit number
- PID System
- Display System
- **Error Signal & Command Input System**

Error Signal & Command Input System

- This system simply takes the input command from the toggles and subtracts off the output of the Encoder-to-RPM block to make an “error signal.”



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Complications

- Low resolution from Encoder-to-RPM block is proving to be quite a problem.
- Proportional control does not correlate very well to Simulink results.
- Preliminary PID controller does not work.
- Lack of one “central” computer to do all work at has slowed progress considerably.

Achievements

- All preliminary VHDL is working.
- Hardware design is completed.
- Motor runs!

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Closing

- We are on schedule.
  - Motor is running.
  - All systems have been designed.
  - In the “test and redesign” phase of project
- We don’t foresee any more obstacles that will prevent us from completing the project successfully.

Questions?