FPGA Implementation of a PID Controller with DC Motor Application

By
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and
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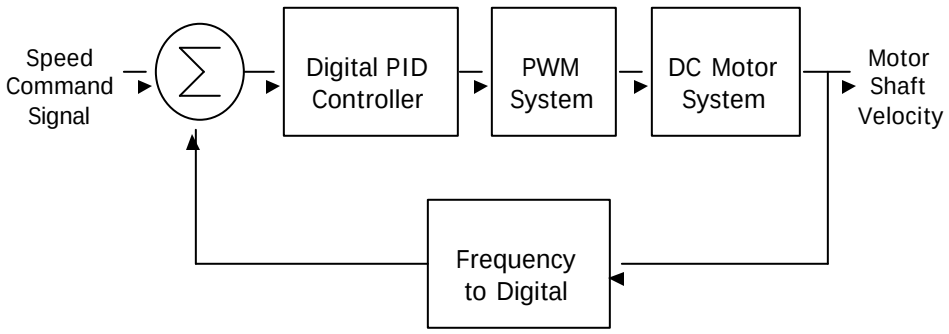
Outline

- Overview and Top-Down Design
- Previous Patents and Standards
- Functional Description
- I/O of Subsystems
- Quantitative Specifications
- Preliminary Lab Work
- Equipment Needed
- Division of Labor

Introduction

- Implementation of a controller in an existing DC motor system
- Minimize cost
- Overcome non-linearity of DC motor
- DC motor speed variations

Top-Down Design



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Previous Work

- Brett Marshall – 2000/2001 Senior Project

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System Inputs and Outputs

Inputs

- Speed Command Signal

Outputs

- Motor Shaft Velocity
- System Display

Modes of Operation

- Full Speed
- Off
- 0 to 800 RPM via user

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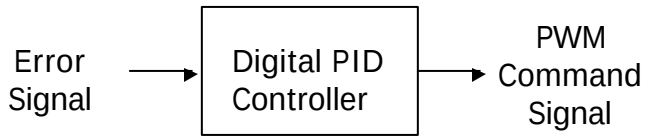
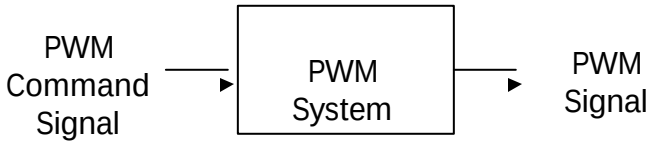
Digital PID Controller



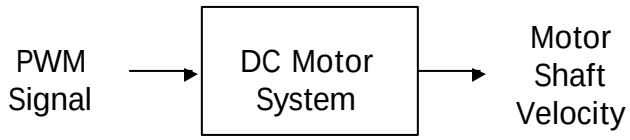
•Error Signal combination of desired input and motor shaft velocity
•PWM Command Signal computed based on Error signal to ensure linearity

PWM System



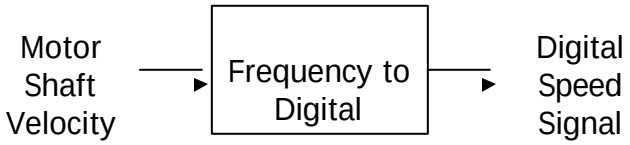
•PWM Command Signal used to create desired percent duty cycled signal

DC Motor System



•PWM Signal used with hardware to control DC Motor System
•Motor Shaft Velocity produced by encoder

Frequency to Digital Converter



•Motor Shaft Velocity sent from encoder on DC motor
•Digital Speed Signal is a digital representation of motor shaft velocity

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Specifications

- Steady State error = 0 for command inputs
- Percent Overshoot = 5%
- Phase Margin > 50 degrees

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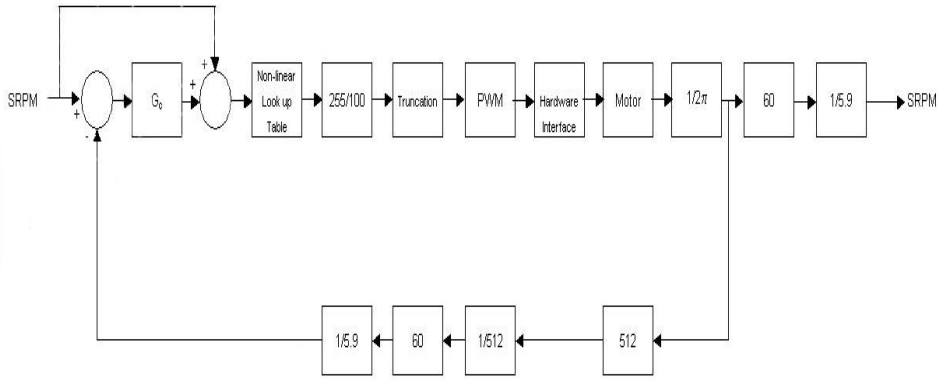
Preliminary Lab Work

- DC Motor Modeling
- PWM System Design
- Complete System Block Diagram
- Investigation of non-linear look-up table implemented in block diagram

Complete System Block Diagram



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Equipment for System

- FPGA Development Board
- Personal Laptops

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Division of Labor

- Due to highly theoretical nature of project, most parts will be completed together.
- *Possible* division of labor:

Paul Leisher	Christopher Meyers
• VHDL Framework	• VHDL PWM Subsystem
• Test System Method and Development	• Reliable Speed Display System