

Bradley University
Senior Project, 2002

FPGA Implementation of a PID Controller with DC Motor Application

System Level Block Diagram

Created By: Paul Leisher
Christopher Meyers

Advised By: Dr. T. Stewart
Dr. G. Dempsey

Last Revised: November 14, 2001

Top-Level System Block Diagram

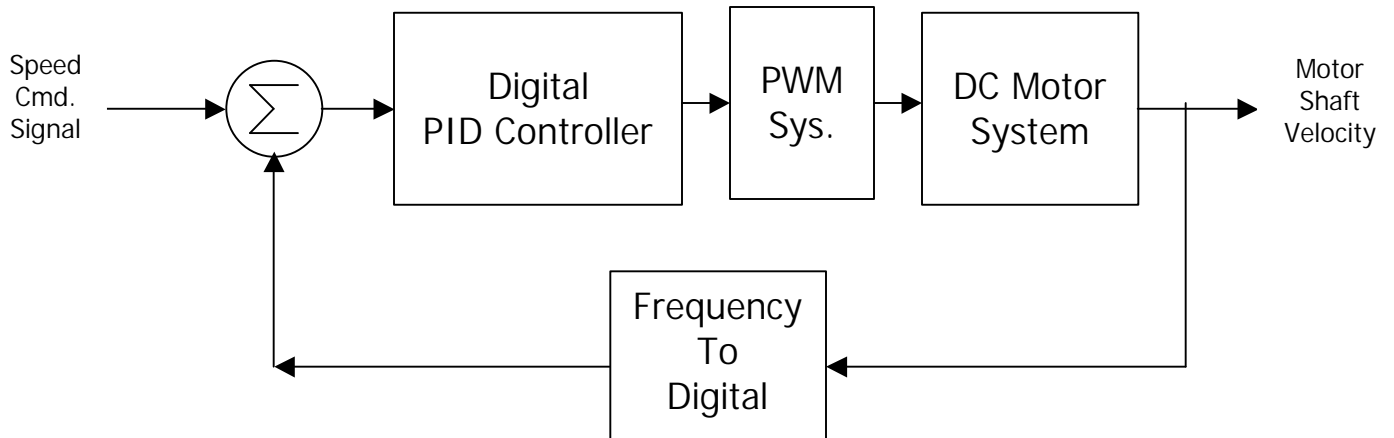


Figure 1:
Top Level Block Diagram

The top-level system block diagram illustrates the Digital PID Controller and DC Motor System in a closed loop configuration. The Motor Shaft Velocity will be fed back and confirmed with the Speed Command Signal to drive the system by means of an error signal. This diagram can be seen in figure 1.

Individual Block Descriptions

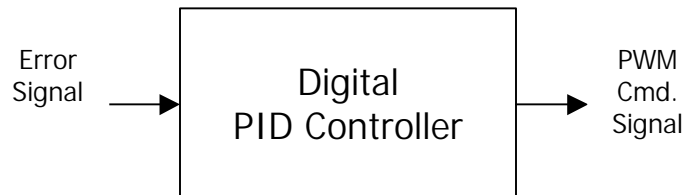


Figure 2:
I/O of Digital PID Controller

The Error Signal is essentially the combination of the desired speed and the motor shaft speed. The PID Controller will use this signal to compute an output signal. The output signal will be the PWM Command signal. The PID Controller will produce the PWM Command signal based on the required input speed and the actual speed of the motor. This will insure that the system is linear with respect to the input speed command signal to the motor shaft velocity. This description can be seen in figure 2.

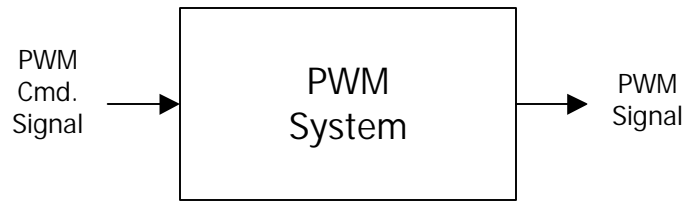


Figure 3:
I/O of PWM System

The PWM System receives a command signal that will then be used to produce the desired percent duty cycled signal that will be the output of this subsystem. The PWM system can be seen in figure 3.

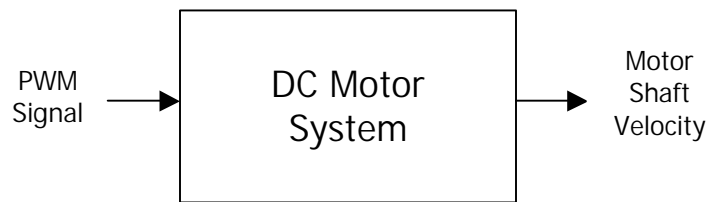


Figure 4:
I/O of DC Motor System

The input to the DC Motor System is a PWM Signal that will be used combined with hardware to control the speed of the motor. The output to this subsystem is a signal generated by an encoder mounted on the rotor of the motor. The encoder produces a signal with the frequency of the signal directly related to the speed of the rotor. The encoder signal will be checked with the desired input speed signal to confirm the motor is at the correct speed. This description can be seen in figure 4.

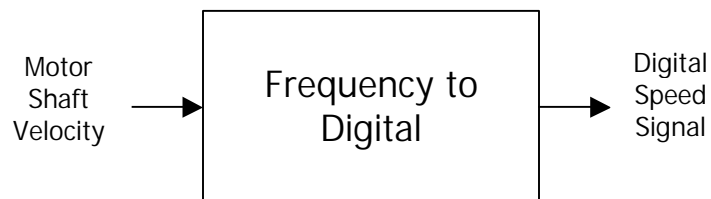


Figure 5:
I/O of Frequency to Digital Converter

The Frequency to Digital Converter takes the motor shaft velocity as an input, which is the signal sent from the encoder on the DC motor. First the signal will be converted to a voltage. This voltage can then be sent through an A/D converter to get digital representation of the motor shaft velocity. This can be seen in figure 5.