Bradley University
Senior Project, 2002

FPGA Implementation of a PID Controller with DC Motor Application

Project Design

Created By: Paul Leisher
Christopher Meyers

Advised By: Dr. T. Stewart
Dr. G. Dempsey

Last Revised: December 13, 2001

Project Summary

In all fields of engineering, many different solutions can be presented for the same problem. The goal of an engineer is twofold. The first and most distinct goal is to identify and design possible solutions to a complex problem. The second goal, which is perhaps less obvious, is to choose which solution is best suitable to most economically meet project specifications. This project deals with the general field of Electrical Engineering. Its primary goal is to implement a digital "Proportional-Integral-Derivative" (or PID) controller in an existing DC motor system with this unwritten economical specification that cost must be minimized.

The existing DC motor system which will be used as our closed loop system "plant" was designed in the Fall 2001 Senior Mini-Project. This system utilized an 80C515 microcontroller to control the speed of a 30-Volt DC motor by pulse width modulation. This system was considered to be an "open-loop" system because no information was fed back to the microprocessor with the express purpose of improving system performance. Two major problems arose due to the open-loop nature of this system. The first problem was system non-linearity that arose due to the nature of the hardware. The second problem was system unreliability when the DC motor load was varied. This project will attempt to address both of these problems by means of a PID controller.

A PID controller, as its name suggests, provides proportional, integral, and derivative compensation to an existing system. These three forms of compensation increase system performance in a variety of ways. Proportional control can both increase gain margin and stabilize a potentially unstable system. Integral control can minimize steady state error. Derivative control can increase system speed by increasing system bandwidth. One drawback of PID control is overall complexity. This results in very expensive means of implementing a digital version of a PID controller. Of the many possibilities, digital signal processors (or DSP's) are the most widely used to solve this problem, however other possibilities exist which may be more cost-effective.

Implementation of any complex digital controller must be done by means of some form of computer. Typical microcontrollers, while cheap, do not normally provide enough processing power to effectively perform all but the most simple calculations real-time. Digital signal processors, on the other hand, are designed to implement complex algorithms quickly. The major drawback of DSP's, however, is cost. This project will attempt to find a median between these two extremes of performance and cost. The proposed solution is to design a special-purpose computer whose only purpose is to quickly execute the complex PID algorithm. This computer will be designed using the IEEE 1076-1987 standard known as VHDL (or Very High Speed Integrated Circuit Hardware Description Language), and will be implemented on an FPGA (or Field Programmable Gate Array).

Detailed Description

The top-level system block diagram illustrates the Digital PID Controller and DC Motor System in a closed loop configuration. The Motor Shaft Velocity will be fed back and confirmed with the Speed Command Signal to drive the system by means of an error signal. This is shown in Figure #1:

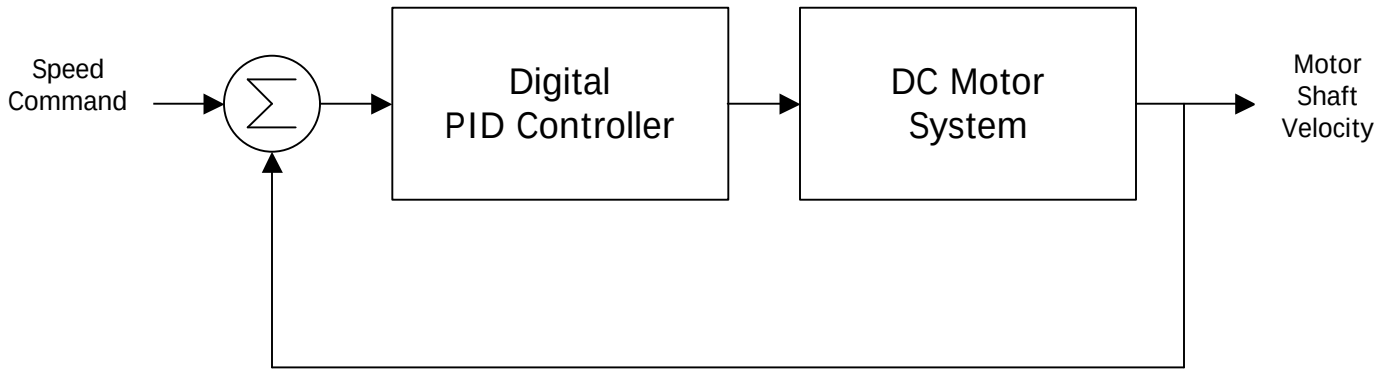

Figure #1: Top-Level Block Diagram

The FPGA, or Field Programmable Gate Array, will be performing a number of tasks in the system. These tasks include processing the Speed Command Input, outputting a DC voltage level drive signal for the DC Motor (this DC voltage level may require further amplification depending on the specifications of the D/A converter included on the FPGA development board), processing the DC Motor RPM encoder's frequency, providing the comparator to compare the Speed Command Input to the Motor Shaft Velocity signal (thus producing an error signal), and the actual implementation of the Digital PID Controller. All of these tasks will be programmed for the FPGA in VHDL. The DC Motor system will be controlled with a DC voltage level. This DC voltage level will be produced on the outputs of the FPGA development board.

The purpose of the proportional gain in the digital PID controller is to provide high loop gain in the system. This high loop gain is crucial to the operation of a closed loop system. Ideally, the system output should follow the system input. For this ideal case, the loop gain would be infinity. However, the proportional gain cannot be made arbitrarily large. What limits this is the FPGA (and the software). The higher the proportional gain, the larger the working numbers in the software will become. At some point, the hardware will not be able to handle such large numbers, and software overflow will occur. This is the first issue which will be addressed in the detailed design of the project, that is, a reasonable balance between the desire for high loop gain and the importance of using smaller numbers will be found. The purpose of the integrator in the digital PID controller will be to

eliminate steady state error. The number of integrators actually implemented in software will depend largely upon how the system will need to track different changes in speed. This system is primarily concerned with tracking step up or step down inputs, so only one integrator will be required. The purpose of the differentiator in the digital PID controller will be to increase system speed by increasing the bandwidth. The functionality of the PID controller on the system is shown in a root-locus sketch below in Figure #2:

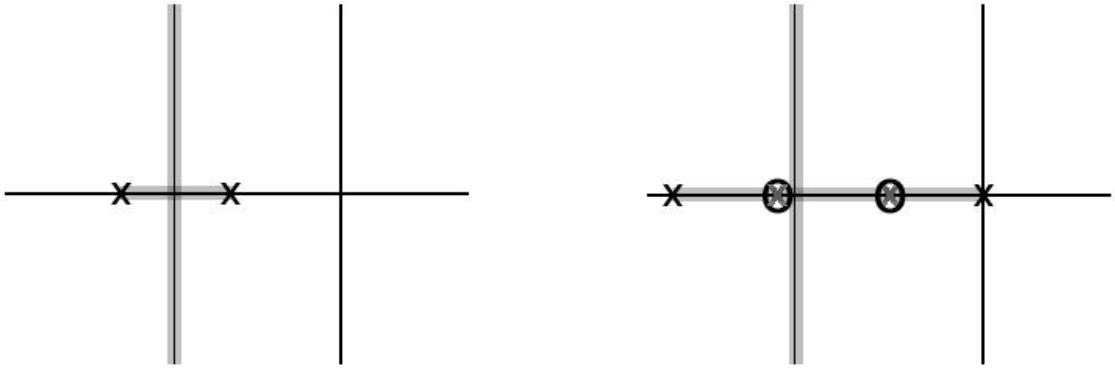

Figure #2: Impact of PID Controller on DC Motor Systems

This project will follow a strict outline of design procedures. The first step will be system simulation. This will be done in Matlab – Simulink. The simulations will be crucial to developing appropriate PID constants for desired system specifications. Although this project will not result in a practical system for direct implementation in industry, a few specifications have been laid down for "academic" purposes. These specifications are listed below:

1. Steady State Error = 0% for command inputs
2. Percent Overshoot = 5%
3. Phase Margin > 50°

The second step will be to develop the software for the FPGA, this includes debugging. The software will be developed based off the design obtained through simulation. Once the software has been designed, it will be implemented on the FPGA, and the system will be operational for testing. From this point on, the goal will be to both improve system performance by "tweaking" the software or by changing the PID parameters, and also to add features to the project by exploring other possibilities. One possibility will be to change the DC Motor System block to input a PWM signal rather than a DC level. Another possibility will be to attempt to add feed-forward control to improve system performance.

Tentative Schedule for Second Semester

Week	Goals
1	Complete initial design simulations
2	Investigate PID Controller configurations and parameters
3	Begin VHDL Software development
4	Finish VHDL Software development
5	Re-evaluate PID parameters as needed for software
6	Design any hardware interfacing
7	Finalize PID parameters in software
8	System testing
9	Design / Implement / Test additional features
10	Design / Implement / Test additional features
11	Design / Implement / Test additional features
12	Finish up; begin project presentation
13	Work on project presentation; begin final report
14	Finish project presentation, and deliver; finish final report
15	Tech Expo

All parts of this project will be worked on together, with the exception of the design, implementation, and testing of additional features. As of now, no additional features have been explicitly planned, so no partner assignments have been made. As time goes on, and more of the project has been completed, this schedule will be updated to include the partner assignments for additional features.

Bibliography

No applicable patents to this project have been found yet.

This project will utilize the FPGA development board designed by Brett Marshall and Mike Parker as their 2000/2001 Senior Project.
Project Site: http://cegt201.bradley.edu/projects/proj2001/xlnxeval/

Equipment List

- Personal laptops
- Matlab v6.0 w/ Simulink
- Expansion Board for Xilinx XS40 FPGA