Hardware Intelligent Control System

By

Brett Ferlin

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Dr. Winfred Anakwa

EE 451 Senior Laboratory

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The proposed project, ‘Hardware Intelligent Control System’, is to create a control system that can adapt to changes in stimulus, be efficient, cost effective, and reliable. In order to create a system that is adaptive and simple it must be able to look up computations quickly. A good application of this project would be in robot control or any sort of adaptive control. A total system diagram would have the basic shape of that shown in figure 1.

The Dark Gray input/output is a bus of indeterminate length. The input sources and outputs can be any sort of port that has access to write to the memory space, and will have respective circuitry to interface them to the memory space depending on application. Example input could be a camera interface that might write a certain range of memory with information of the current camera view. Example output may be some memory that the output circuitry will interpret as a motor movement in some direction.

This is a proposed system, because it is very theoretical at this time. Because of the modular nature of this project, it is uncertain the viability or efficiency nor what the final circuit will resemble. Figure 1 also represents a state diagram of sorts. The actual work is completely done by the so-called “Neuron chips”. The microprocessor simply copies information from the memory space to the “Neuron chips” and back following the arrow around. It also will have some sort of programming functions to reprogram the chips dynamically. This is shown through the small control lines shown to go to each neuron chip. Each “Neuron chip” should resemble the block diagram shown in Figure 2.
The basic operation of any given chip would be to check the input bus (of indeterminate length) for some given input word. It is compared with the number stored in the flip-flop. If this number is found to be the same, the output is switched from the input to the second flip-flop, which contains the response word for the input. In this manner, it is hoped to mirror the efficiency of biological neurons at looking up response data as quickly as possible with as little cost in time as possible. The data storage method for the ‘memory space’ should allow it to evolve the method of solving problems as well as returning data for use in whatever responses are necessary. So far, a description of the memory space seems to be that shown in Figure 3.

The Control word and Data section is of undetermined size. When it is determined the most efficient number of neuron chips and their corresponding pins for this project, this size will be chosen. A single cycle of this system should take some part of the memory space, copy it to the bus and read the output. It should then parse the control word and act accordingly with the data. Then the cycle starts over again. It will be likely that all system components might be redesigned a few times before finding a useful configuration, however this functional description gives the basic idea.