DATA MOVER USING VLSI

By: Ricardo V. Gonzalez
Advisor : Vinod B. Prasad

December 11, 2000

PROJECT SUMMARY

The purpose of this project is to build a Data Mover of 4 bits, testing first a Data Mover design of 2-bits. This project will be implemented using VLSI and will be tested using Logic Works and Mentor Graphics.

The paramount importance of this project is to create the possibility of moving data from one input to multiple outputs at a much higher speed also to multiply the number of users in computer terminals or multiplexing the output signal of a receiver to multiple decoders. Many more applications can be found to this device.

DETAILED DESCRIPTION

The Data Mover will be designed first using the theory of RTL (Register Transfer Language). The device will be implemented for testing purposes using Logic Works. The ultimate goal is to build it into an actual chip so it has to be implemented using VLSI. The logic gates have to be designed and tested individually prior merging with the final project. A multiplexer or a sequence generator will control the operation of the Data Mover. A Data Mover of 4 bit needs 16 memory blocks that will be implemented using D flip-flops for data analysis and process. A 2 bits Data Mover will be implemented first for simplistic reasons. The device will need a master clock, which will provide the speed and timing necessary for the appropriate operation of the Data Mover. This design will also avoid the propagation of data error, which is a very valuable feature.

The following are descriptions of the elements of the graph 1 " **BLOCK DIAGRAM":**

A) INPUT The input will be 4 bits from an external source. The test bits can be known to the user to ensure proper performance.

B) CIRCUIT CONTROLLER

The circuit controller will be one of the two possibilities: a multiplexer or a sequence generator.

C) ALGORITHM CIRCUIT

The algorithm circuit will be designed using RTL (Register Transfer Language). The algorithm is in charge of manipulating the data.

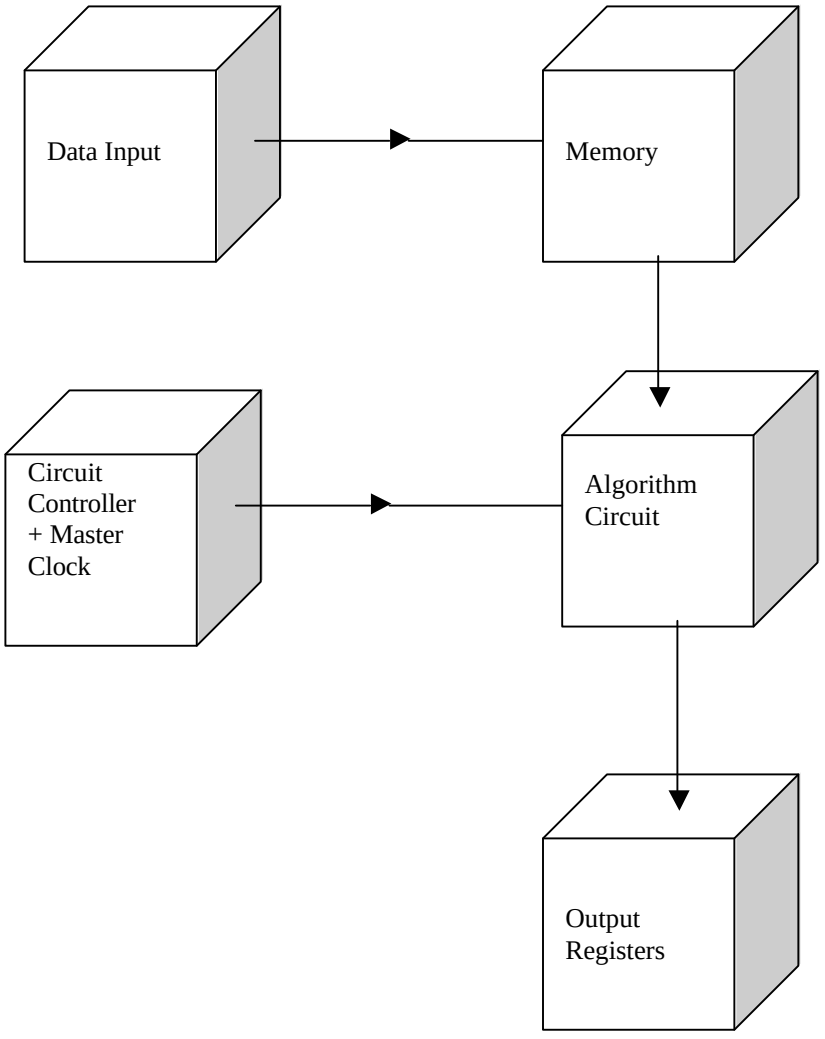
D) SEQUENCE GENERATOR

The sequence generator will be the circuit commanding the algorithm circuit the timing of data transferring operations. This circuit still being debated if will be an arrangement of memory registers or a multiplexer.

E) OUTPUT REGISTER

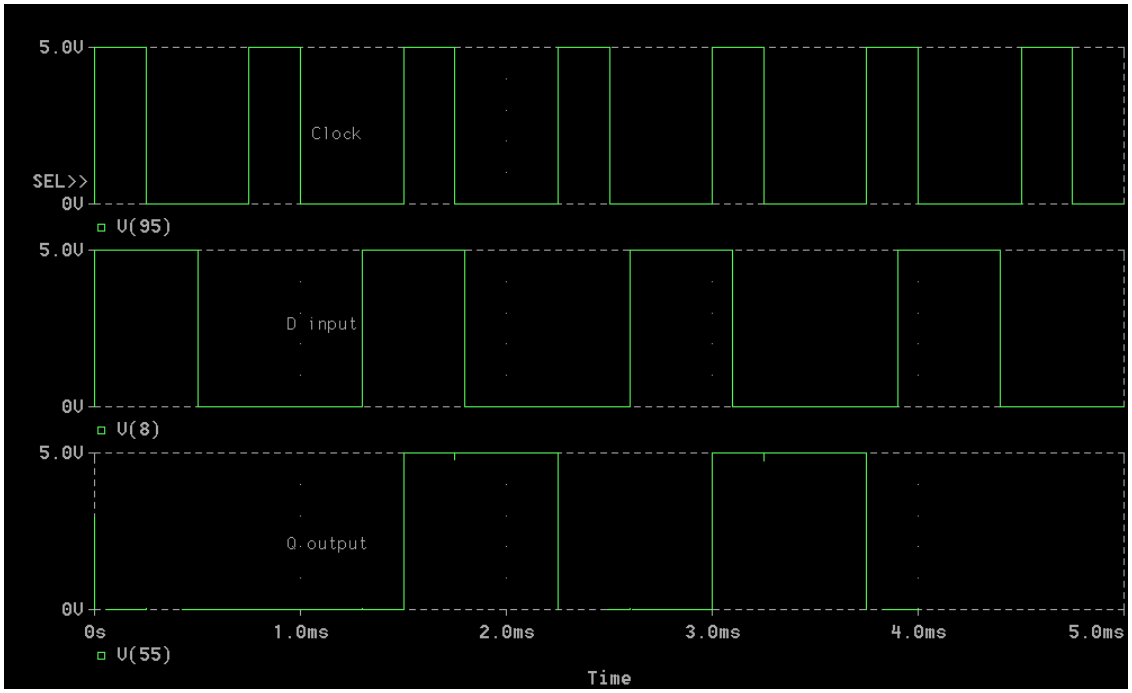
The output register will be an organized set of D flip-flops to hold the data for proper analysis and process.

Graph 1 “Block Diagram”



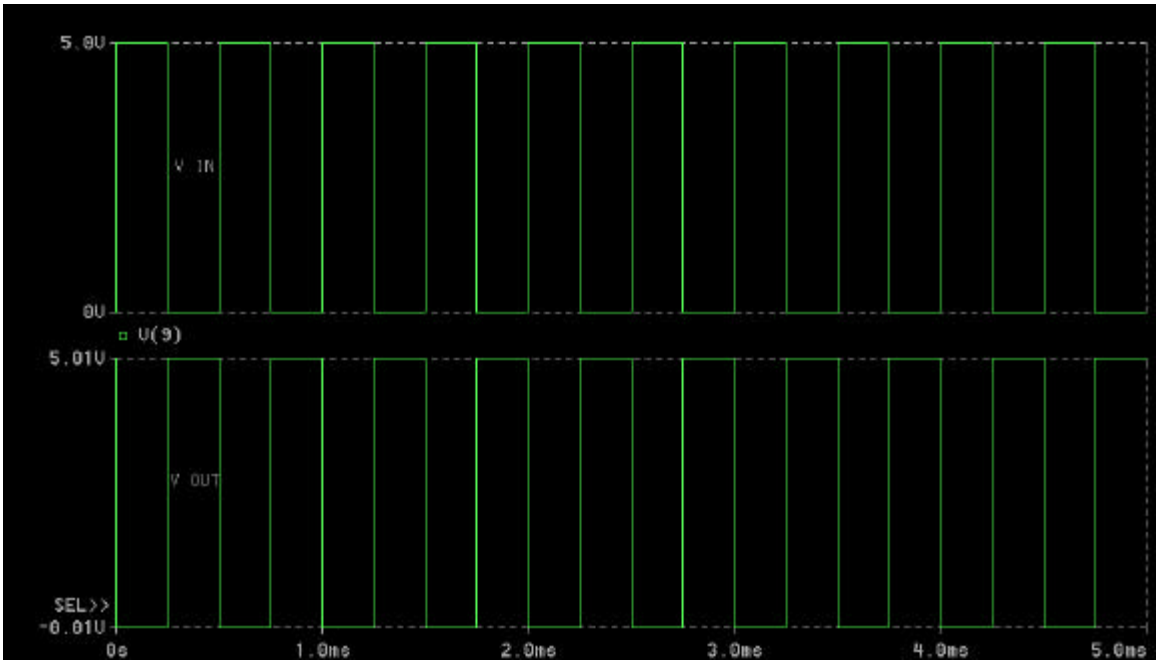
The following graphs are computer simulations of gates finished in VLSI.

Graph 2 “D flip-flop”

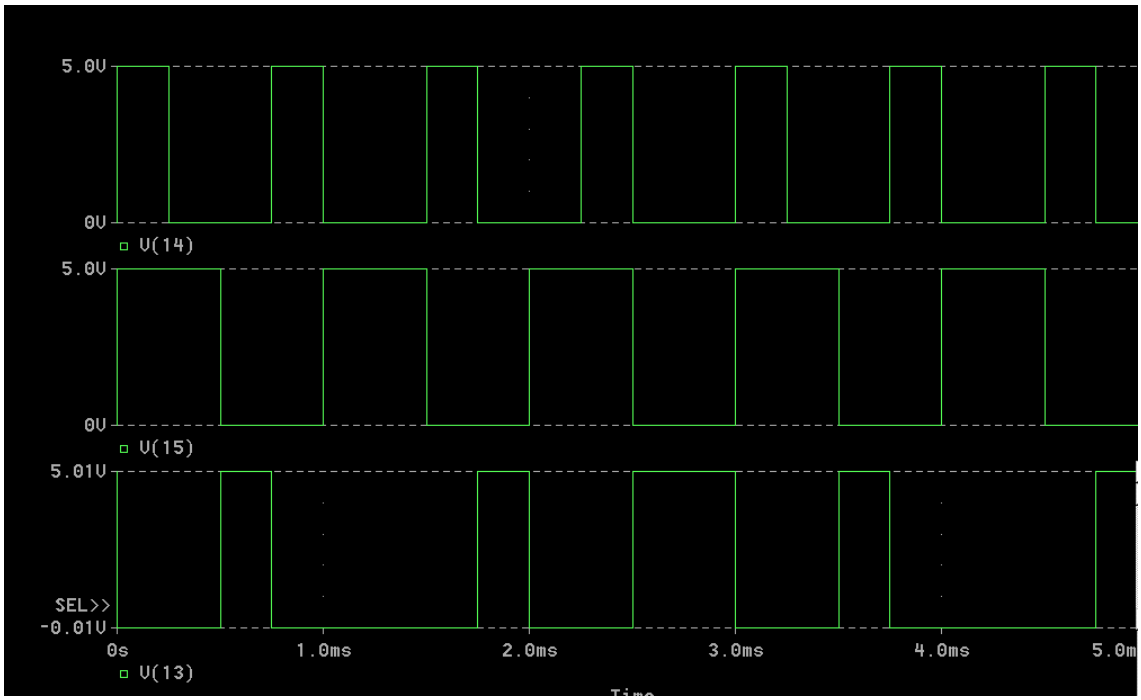


D flip-flop simulated in Pspice.

Graph 3 “Inverter Simulation”

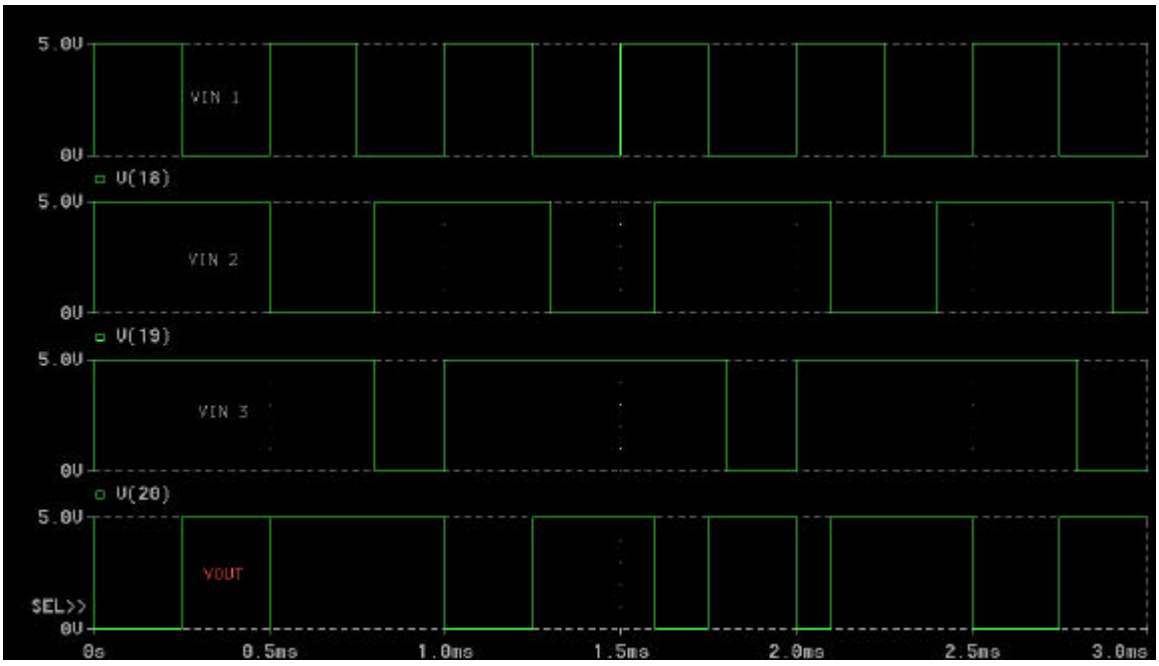


Graph 4 “Nor Gate computer simulation”



Nor Gate simulation in Pspice. Having node V(14) and V(15) as the inputs and node V(13) as the output.

Graph 5 “Nand Gate Computer Simulation”



Logic Works will simulate the circuit as a whole that is most of the circuit implemented.
Pspice will do the simulation in the transitor level of the CMOS gates done in LEDIT.
Pspice will show the final result of the computer simulation.

SCHEDULE

Tasks already done	Tasks to be completed
-Simulation of the Data Mover in Logic Works. -Design of NAND gate in LEDIT with proper simulation in Pspice. -Designed Inverter in LEDIT with proper simulation in Pspice. - Designed D flip-flop in LEDIT and simulated also in Pspice. -Designed in Logic Works Algorithm Circuit. -Implemented in Logic Works Circuit Controller.	-Week 1: Re-design D flip-flop in LEDIT to to make it more compact and simulated in Pspice. -Week 2: Design circuit controller in LEDIT with proper simulation. -Week 3: Design algorithm circuit for two bits. -Week 4: Implement algorithm circuit for four bits. -Week 5: Simulate algorithm circuit for two bits. -Week 6: Simulate algorithm circuit for four bits. -Week 7: Research creative production. -Week 8: Continue research of creative production. -Week 9: Continue research of creative production. -Week 10: Start work for production exhibition. -Week 11: Continue work for production exhibition. - Week 12: Start work for presentation. -Week 13: Continue work for presentation. -Week 14: Finalize work for final presentation. -Week 15: I better have everything ready for presentation and student exposition.

REFERENCES

MOSIS: Some design rules provided by the MOSIS program (i.e. transistor Models)

Mukherjee, Amar. Introduction to NMOS & CMOS VLSI system design. New P.T.R Prentice Hall, Inc 1986

Uyemura, John P. Physical Design of CMOS Integrated Circuits Using L-EDIT Boston PWS Publishing Company.