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DATA MOVER DESIGN USING VLSI

FUNCTIONAL DESCRIPTION

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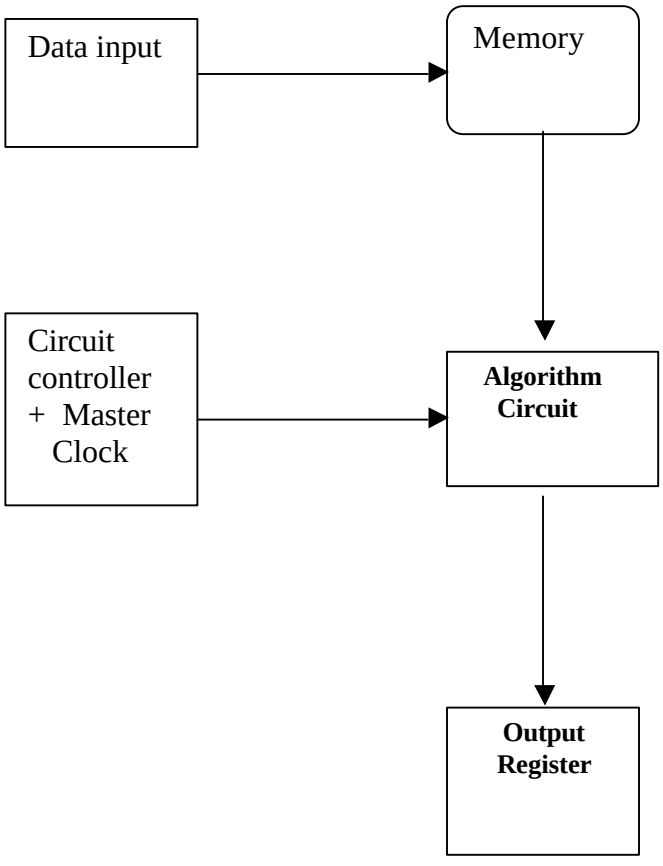
The main objective is to design a device that will create the possibility of moving the data input to multiple outputs. An input of 4 bits will be the entering data to test the operability of the chip. The Data Mover is an independent customized communication algorithm in a variety of block structured applications. The Data mover enables the user to express data motion using intuitive geometric operations. The chip will serve as a useful middleware for multiple users if multiple chips are implemented.

The chip will be simulated first in Logic Works and then implemented in VLSI. A multiplexer or a sequence generator will control the operation of the chip. The memory block will be 8 D-flip flops. They will hold the data for analysis and process. A master clock will drive the chip. The Data Mover also will avoid the propagation of error in any data input to the output.

Figure 1. **Data Mover Block Diagram**.



The following is a description of the corresponding labels from the block diagram.

A) INPUT

The input will be 4 bits from an external source. The test data will be known to the user to ensure proper effectiveness.

B) CIRCUIT CONTROLLER

The circuit controller will be a logic arrangement following a convenient algorithm. The circuit controller will be a set of gates that manipulates the data.

C) ALGORITHM CIRCUIT

This circuit is used to manipulate data following an algorithm.

D) SEQUENCE GENERATOR

This function is reserved for a master clock. This clock will control the registers and the logic arrangement.

E) OUTPUT REGISTERS

The four-bit output will be held in the output register for convenient check up of the output data.