

DATA MOVER DESIGN USING VLSI

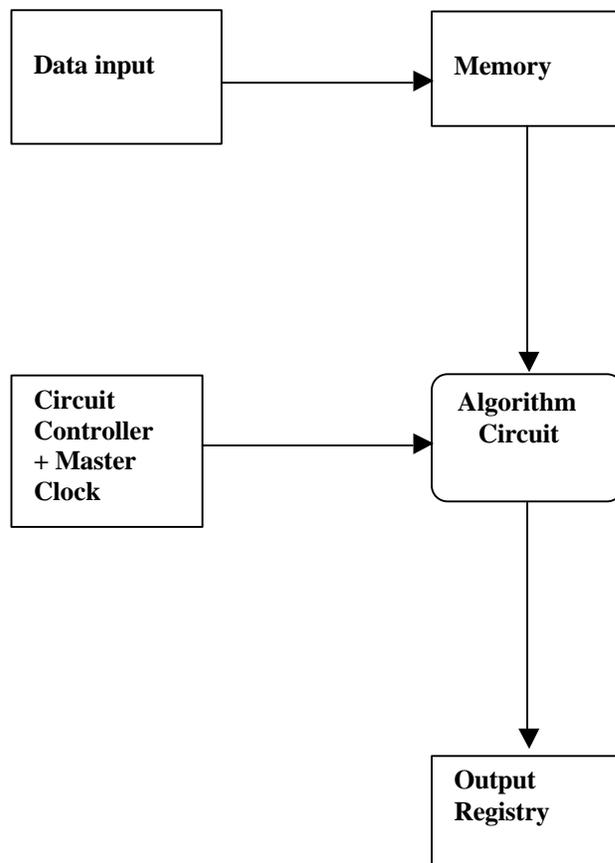
BLOCK DIAGRAM

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The project Data Mover Design using VLSI will be the actual creation of a chip that will produce the image of the data at the output. Also will reduce the possibility of error propagation in the data output. Multiple chips will create the possibility of reproducing the information multiple times for multiple users at a higher data rate transfer.

The main components of the Data Mover are shown in Figure 1. The Data Mover Block Diagram. The data input, memory, a block controller and the output registry.

Figure 1. Data Mover Block Diagram.



- **The input will be external data that could be a computer information, data received from a transmission channel, etc.**
- **Memory: Memory will be the implementation of D flip-flops.**
- **The circuit controller: will be a logic system that checks the data and manipulates the data before goes to the Output registry.**
- **The output registry is the block where the data is checked and corrected with the help of the circuit controller to reduce to the minimum possible errors.**

The system will be first simulated using logic works and Mentor Graphics. After the circuit is checked with simulation the chip will be realized in VLSI .

This circuit could be used to multiply the number of users in a computer network where multiple users are working at the same time at a higher speed. Also, to record massive tapes, and to act as a data buffer to burn multiple compact discs at the same time much faster. Further applications are still under research.

The components of the memory and controller are still being discussed with the advisor. The number of bits has to be an even number; this will be 4 data bits input. This will make the project fairly complex for the scope of this project.