Active Duplexer
Complete System Level Block Diagram

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I. Overall System Block Diagram

Figure 1 shows the overall PCS (Personal Communication System) block diagram. The active duplexer (AD) referred to in this paper is pointed out with a large arrow. Figure 2 shows the inputs and outputs of the AD. T1 is a signal that is being transmitted by the transceiver before it has been amplified by the AD. R2 is the received signal after it has been amplified by the AD. R1 is the signal received from a different transceiver before it has been amplified by the AD, and T2 is the signal being transmitted by the transceiver after passing through the active duplexer.

II. System Level Block Diagram

The diagram below in Figure 3 is the system level block diagram of the AD. It is devised of two FETs with their gates tied to an artificial transmission line with a characteristic impedance of $Z_g$. The drains are connected similarly to a T-line with a characteristic impedance of $Z_d$. The input signals from Ports 1 and 2 travel along the gate T-line and are then amplified by the FETs. The amplified signal then travels along the drain T-line. The T-lines will be set up so that a signal phase is added for S32 (signal from Port 2 to Port 3) and destructive in the undesired direction, S31. This is desired so that the signal from Port 1 does not enter Port 3. Also of note, S21 (the signal traveling from Port 1 to Port2) experiences an attenuation loss and is not amplified by the FET.
The bias T has been shown in Figure 3, and are used to keep the microwaves off of the DC voltage supply.

Fig. 3 – System Level Block Diagram