Abstract

An active duplexer design concept is presented. The bidirectional amplifier can be realized with the use of GaAs FET’s. The amplifier is used for isolating transmitted and received signals, while applying a gain to the received signal. This paper gives an introduction to active duplexers and discusses the status of the design project.
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I. **Introduction**

The objective of this project will be to design an active duplexer for a wireless CDMA communication system that operates at 1.9GHz. A PCS system already exists in the RF Laboratory and is incorporating an active duplexer, but this project will be to improve the performance of the current design. Other features include a unipolar power supply, bias-T’s incorporated onto the circuit board, and the active duplexer will be packaged in its own chassis.

An active duplexer is a device that makes receiving and transmitting data at the same time possible, from the same antenna. Further it isolates the received and transmitted signals from one another. Unlike passive duplexers, where a low noise amplifier is needed prior to the device to apply a gain to a received signal, an active duplexer applies its own gain.

II. **Functional Description**

![Fig. 1 – Signal paths of the Distributed Amplifier](image)

S32 shows the received signal, the signal will travel from Port 2 to Port 3. S21 is the transmitted signal; this signal travels from Port 1 to Port 2. S31 is the isolation between ports 1 and 3, which should be very low (less than –20dB) for the frequency of operation.

Listed below in Table 1 is the mode of operation and the inputs and outputs of the active duplexer. Use Figure 2 to further observe the Inputs and Outputs of note.
Fig. 2 – Inputs and Outputs of Active Duplexer

<table>
<thead>
<tr>
<th>Transmitting and Receiving</th>
<th>Function</th>
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<tbody>
<tr>
<td>Transmit Signal (T1)</td>
<td>This is the signal that will be transmitted from the transmitter prior to manipulation from the active duplexer.</td>
</tr>
<tr>
<td>Received Signal (R1)</td>
<td>This is the signal that will be received from another transmitter prior to manipulation from the active duplexer.</td>
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</table>

<table>
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<tr>
<th>Outputs</th>
<th>Function</th>
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<tbody>
<tr>
<td>Transmit Signal (T2)</td>
<td>This is the signal that will be transmitted from the transmitter after manipulation from the active duplexer.</td>
</tr>
<tr>
<td>Received Signal (R2)</td>
<td>This is the signal that will be received from another transmitter after manipulation from the active duplexer.</td>
</tr>
</tbody>
</table>

### III. Block Diagrams

Figure 3 shows the overall PCS (Personal Communication System) block diagram. The active duplexer referred to in this paper is pointed out with a large arrow.

The diagram below in Figure 4 is the system level block diagram of the active duplexer. It is devised of two FETs with their gates tied to an artificial transmission line with a characteristic impedance of $Z_g$. The drains are connected similarly to a T-line with a characteristic impedance of $Z_d$. The input signals from Ports 1 and 2 travel along the gate T-line and are then amplified by the FETs. The amplified signal then travels along the
drain T-line. The T-lines will be set up so that a signal phase is added for S32 (signal from Port 2 to Port 3) and destructive in the undesired direction, S31. This is desired so that the signal from Port 1 does not enter Port 3. Also of note, S21 (the signal traveling from Port 1 to Port 2) experiences an attenuation loss and is not amplified by the FET.

The bias T has been shown in Figure 4, and are used to keep the microwaves out of the DC voltage supply.

![Impedance Matching Networks](image)

**Fig. 4 – System Level Block Diagram**

The propagation constants of the gate and drain line are chosen for constructive interference for signals in the desired direction and destructive interference in the undesired direction.

There are two signals that appear at the drain of Amp 1: a wave which undergoes a phase shift of \(-\alpha\), from Amp 1, and travels toward Port 3, and another traveling wave which goes through Amp 2 with a phase shift of \((-180^\circ - \alpha)\). Since the two waves are 180\(^\circ\) out of phase with one another, they cancel. There are also two signals present at the drain of Amp 2. One is the forward traveling wave which undergoes a phase shift of \(90^\circ - \alpha\) through Amp 1, and the second is a forward traveling wave that goes through a phase shift of \(90^\circ - \alpha\) from Amp 2. These two signals are added in a constructive manner. Refer to Figure 5 for guidance.
Typically a FET is biased using two power supplies, one for the gate and one for the drain. This active duplexer will incorporate a unipolar power supply, which allows for just one DC power supply. This is accomplished by attaching a resistor from source to ground (Refer to Figure 6). $I_{DS}$ will pass through this resistor causing a voltage drop. This keeps the gate at a negative potential with respect to the source. There is a large capacitor in parallel with the resistor that is used to bypass RF to ground. The inductor connected to the gate is used to offer a low impedance to DC but a very high impedance to RF, thus eliminating any AC feedback.
A bias-T will be designed to keep RF off of the DC power supply voltage, and will be fabricated onto the circuit board. The bias-T or choke network consists of a large capacitor to ground that shorts RF to ground and a quarter wavelength microstrip that is connected to the drain of the FET. This quarter wavelength microstrip will offer a large impedance to RF but should have no significant affect on DC. Refer to Figure 7 for a diagram of the choke network.

![Diagram of Choke Network](image)

**Fig. 7 – Choke network diagram**

IV. **Datasheet**

**Design Goal Specifications:**

- Bandwidth: 1850MHz to 1990MHz
- Isolation (S31 crosstalk) > 20dB attenuation
- Forward Transmission Coefficient (S21) < 2dB attenuation
- Forward Transmission Coefficient (S32) > 7.5dB
- Reflection Coefficient at Port 1 (S11) < -12dB
- Reflection Coefficient at Port 2 (S22) < -20dB

**Features:**

- Bidirectional Amplifier
- Unipolar (One source) power supply
- Metal Enclosure with SMA connectors
- Bias-T network is incorporated onto the circuit board
- Only 14mW of power consumption

V. **Preliminary Lab Work**

Preliminary Lab work has consisted of working on research, design and simulation of bidirectional amplifiers. Currently a design does exist that applies a gain to a received signal, but does not isolate the transmitted and received signals from each other by the
use of phase cancellation. Also a preliminary choke network has been designed for biasing the FET’s. Design considerations have also been made taking into account the metal enclosure.

VI. Important Design Equations

The following equation is used to determine the cutoff frequency of the amplifier taking into account the phase shifting networks.

$$\theta = m \cos^{-1}[1 - 2\omega^2/\omega_c^2]$$

where, $\theta$ is the phase shift of 90°, $\omega_c$ is the cutoff frequency of the gate and drain lines, and $m$ is the number of phase shifting networks. Solving the above equation for $f_c$,

$$45 = \cos^{-1}[1 - 2*(1.9*10^6)^2/f_c^2]$$

$f_c = 4.96$GHz.

Using the equation,

$$R_1 = (L_g/C_{in})^{-1/2}$$

where $C_{in}$ is the capacitance looking into the FET, $L_g$ is the gate line inductance, and $R_1$ is the gate line characteristic impedance, and the equation,

$$f_c = 1/\pi * (L_g * C_{in})^{-1/2}$$

it is possible to solve for $L_g$. Similar calculations can be made for obtaining $L_d$, by substituting $L_d$ and $C_{out}$ into the previous two equations.

VII. Equipment List

- Network Analyzer – for circuit measurements
- HPEEsof – for design simulation
- Spectrum Analyzer – for circuit measurements
- DC Power Supply – to supply a DC voltage to the FET’s
- Fabrication Laboratory – to physically construct the circuit
VIII. Schedule for Spring 2000

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Bibliography


