SYSTEM BLOCK DIAGRAM

The main objective is to design testability features that can potentially be included in any CMOS chip. A 4-bit x 4-bit multiplier will be the circuit used to test the designed testability features. The VLSI design of the 4-bit x 4-bit multiplier circuit will contain sixteen cells. The testing features consist of a sequence generator and 8-bit registers for a signature analysis. The multiplier will have a total of eight inputs and eight outputs. The sequence generator, controlled by a clock and a start bit, will be used for cellular testing. The outputs of the sequence generator will be given to the user. Therefore, the expected outputs of the multiplier will also be known to the user based upon the multiplier truth table. The 8-bit registers will be used to store the information provided from the test. Outputs will also come from the registers for easy observation of the test's results.

The following are descriptions of the corresponding labels for the **BLOCK DIAGRAM**:

CELLS 1 THROUGH 16

These sixteen identical cells are the basis of the 4-bit x 4-bit multiplier circuit. These cells will be designed using basic CMOS techniques.

A) 4 x 4 MULTIPLIER INPUTS

These are the external inputs to the 4-bit x 4-bit multiplier circuit. These connections will also be used internally as the inputs from the sequence generator to test the function of the 4 x 4 multiplier when the chip is in test mode.

B) 4 x 4 MULTIPLIER OUTPUTS

These pins are reserved for the outputs of the 4-bit x 4-bit multiplier circuit. These connections are also used internally to supply an input to the registers when the chip is in test mode.

C) SEQUENCE GENERATOR START BIT

When set, the chip will begin its own diagnostic functions which will consist of a series of 8-bit words, known to the user, sent from the sequence generator to the inputs of the 4-bit x 4-bit multiplier. The external inputs and outputs will be disregarded.

D) SEQUENCE GENERATOR CLOCK

This pin is reserved for an external clock. This clock drives the sequence generator and the registers.

E) SEQUENCE GENERATOR OUTPUTS

These outputs will consist of 8-bit words used as inputs for the 4-bit x 4-bit multiplier when the chip is in test mode. These outputs will be given to the user. The sequence generator will be designed using CMOS techniques.

F) REGISTER INPUTS

The 8-bit registers are used to store the outputs from the 4-bit x 4-bit multiplier when the chip is in test mode. The user will know the inputs from the sequence generator to the mulitplier, and therefore will also know the expected outputs from the multiplier. The outputs from the multiplier are stored in registers because the test verifies many different outputs based upon many different input combinations. Since the test is clock driven the registers allow for easy viewing of multiple test results. The registers will also be designed using CMOS techniques.

G) REGISTER OUTPUTS

Comparing these outputs with the expected outputs from the 4 x 4 multiplier will give the results of the test.

H) VOLTAGE SUPPLY

I) GROUND

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TESTABLE VLSI CIRCUIT DESIGN FOR CELLULAR ARRAYS

BLOCK DIAGRAM