Jarrod Luker
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SENIOR DESIGN PROJECT PROPOSAL

Jarrod Luker **Tim McKinney**

TESTABLE VLSI CIRCUIT DESIGN FOR CELLULAR ARRAYS

PROJECT SUMMARY

The main objective of this project is to design testability features that can potentially be included in any CMOS chip. For this particular design a 4-bit x 4-bit multiplier will be the circuit used to test the designed testability features.

The relevance of this project is not to test the cells of a 4-bit x 4-bit multiplier or a 4-bit x 4-bit multiplier itself. The purpose of this project is to design a system that can be fabricated on a chip so that the main function of that chip can be tested with a minimal amount of external hardware or software.

Testability of a chip plays a key role in the use and repair of PCBs. If a single button can be pushed to test a chip on a board, then a very powerful tool has been created. If on-chip testing features "say" a chip is bad, then only that chip needs to be replaced, not the entire PCB.

Again the purpose of this project is to develop an easy method for finding a bad chip, not to test a single cell of a cellular array.

DETAILED DESCRIPTION

The VLSI design of the 4-bit x 4-bit multiplier circuit will contain sixteen cells. The testing features consist of a sequence generator and an 8-bit register for a signature analysis. The multiplier will have a total of eight inputs and eight outputs. The sequence generator, controlled by a clock and a start bit, will be used for cellular testing. The outputs of the sequence generator will be given to the user. Therefore, the user will know the expected outputs of the multiplier based upon the multiplier truth table. The 8-bit register will be used to store the information provided from the test. Outputs will also come from the register for easy observation of the test's results. The importance of this project is to show the amount of hardware that could potentially be needed to fully test a chip, and reduce that hardware by implementing VLSI and digital design rules to develop on-chip testing features.

The following are descriptions of the corresponding labels for the **BLOCK DIAGRAM**:

CELLS 1 THROUGH 16

These sixteen identical cells are the basis of the 4-bit x 4-bit multiplier circuit. These cells will be designed using basic CMOS techniques.

A) 4 x 4 MULTIPLIER INPUTS

These are the external inputs to the 4-bit x 4-bit multiplier circuit. These connections will also be used internally as the inputs from the sequence generator to test the function of the 4 x 4 multiplier when the chip is in test mode.

B) 4 x 4 MULTIPLIER OUTPUTS

These pins are reserved for the outputs of the 4-bit x 4-bit multiplier circuit. These connections are also used internally to supply an input to the registers when the chip is in test mode.

C) SEQUENCE GENERATOR START BIT

When set, the chip will begin its own diagnostic functions which will consist of a series of 8-bit words, known to the user, sent from the sequence generator to the inputs of the 4-bit x 4-bit multiplier. The external inputs and outputs will be disregarded.

D) SEQUENCE GENERATOR CLOCK

This pin is reserved for an external clock. This clock drives the sequence generator and the registers.

E) SEQUENCE GENERATOR OUTPUTS

These outputs will consist of 8-bit words used as inputs for the 4-bit x 4-bit multiplier when the chip is in test mode. These outputs will be given to the user. The sequence generator will be designed using CMOS techniques.

F) REGISTER INPUTS

The 8-bit register is used to store the outputs from the 4-bit x 4-bit multiplier when the chip is in test mode. The user will know the outputs from the sequence generator to the multiplier, and therefore will also know the expected outputs from the multiplier. The outputs from the multiplier are stored in the register because the test verifies many different outputs based upon many different input combinations. Since the test is clock driven the register allows for easy viewing of multiple test results. The register will also be designed using CMOS techniques.

G) REGISTER OUTPUTS

Comparing these outputs with the expected outputs from the 4 x 4 multiplier will give the results of the test.

H) VOLTAGE SUPPLY

I) GROUND

The **LOGIC WORKS SIMULATION** is an example of pre-design work. Logic Works is used to test a design before proceeding to the CMOS design stage. The **CMOS DESIGN USING L-EDIT** shows the CMOS design stage. This particular design is the final design of the 4-bit x 4-bit multiplier cell. The next design stage is to simulate the CMOS design using PSPICE. The **PSPICE SIMULATION** shows the final simulation of the 4-bit x 4-bit multiplier cell. These three main stages of design will be used throughout the duration of the project.

To test the testability features after the fabrication process the 4-bit x 4-bit multiplier will first be tested manually without the testability features in use. Then the 4-bit x 4-bit multiplier will be tested using the testing features. If the results of the test using the testing features match the results of the manual test of the 4-bit x 4-bit multiplier then the testing features work properly.

SCHEDULE

COMPLETED TASKS:

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• 4-bit x 4-bit multiplier cell designed • CMOS 4-bit x 4-bit multiplier cell designed using L-EDIT • CMOS 4-bit x 4-bit multiplier designed using L-EDIT	• 4-bit x 4-bit multiplier cell designed • 4-bit x 4-bit multiplier simulated using Logic Works • CMOS 4-bit x 4-bit multiplier cell simulated using PSPICE • CMOS 4-bit x 4-bit multiplier simulated using PSPICE

TASKS TO BE COMPLETED:

Jarrod Luker	Tim McKinney
12/03/98 • Design of and Logic Works simulation of sequence generator 01/21/99 • CMOS design of sequence generator 01/28/99 • Continuation of CMOS design of sequence generator 02/04/99 • PSPICE simulation of sequence generator completed 02/11/99 • Finalize completed design to be sent for fabrication on 02/17/98 02/19/99 • Start hardware design for 1999	12/03/98 • Design of and Logic Works simulation of 8-bit register 01/21/99 • CMOS design of 8-bit register 01/28/99 • Continuation of CMOS design of 8-bit register 02/04/99 • PSPICE simulation of 8-bit register completed 02/11/99 • Finalize completed design to be sent for fabrication on 02/17/98 02/19/99 • Start hardware design for 1999

Research/Creative Production Exhibition	Research/Creative Production Exhibition
02/26/99	02/26/99
• Continue work for Production Exhibition	• Continue work for Production Exhibition
03/05/99	03/05/99
• Continue work for Production Exhibition	• Continue work for Production Exhibition
03/12/99	03/12/99
• Continue work for Production Exhibition	• Continue work for Production Exhibition
03/19/99	03/19/99
• Continue work for Production Exhibition	• Continue work for Production Exhibition
03/26/99	03/26/99
• Continue work for Production Exhibition	• Continue work for Production Exhibition
04/02/99	04/02/99
• Finalize work for Production Exhibition	• Finalize work for Production Exhibition
04/09/99	04/09/99
• Begin work on final presentation	• Begin work on final report
04/16/99	04/16/99
• Continue work on final presentation	• Continue work on final report
04/23/99	04/23/99
• Continue work on final presentation	• Continue work on final report
04/30/99	04/30/99
• Finalize final presentation	• Finalize final report

REFERENCES

MOSIS Program. Some design rules provided by the MOSIS Program (i.e. transistor models)

Mukherjee, Amar. Introduction to NMOS & CMOS VLSI Systems Design. New Jersey: P T R Prentice-Hall, Inc. 1986.

Prasad, Dr. V. In order to increase the chances of a successful fabrication, Dr. V. Prasad has supplied previously tested and fabricated logic gates for use in this design.

Uyemura, John P. Physical Design of CMOS Integrated Circuits Using **L-EDIT**™. Boston: PWS Publishing Company. 1995.

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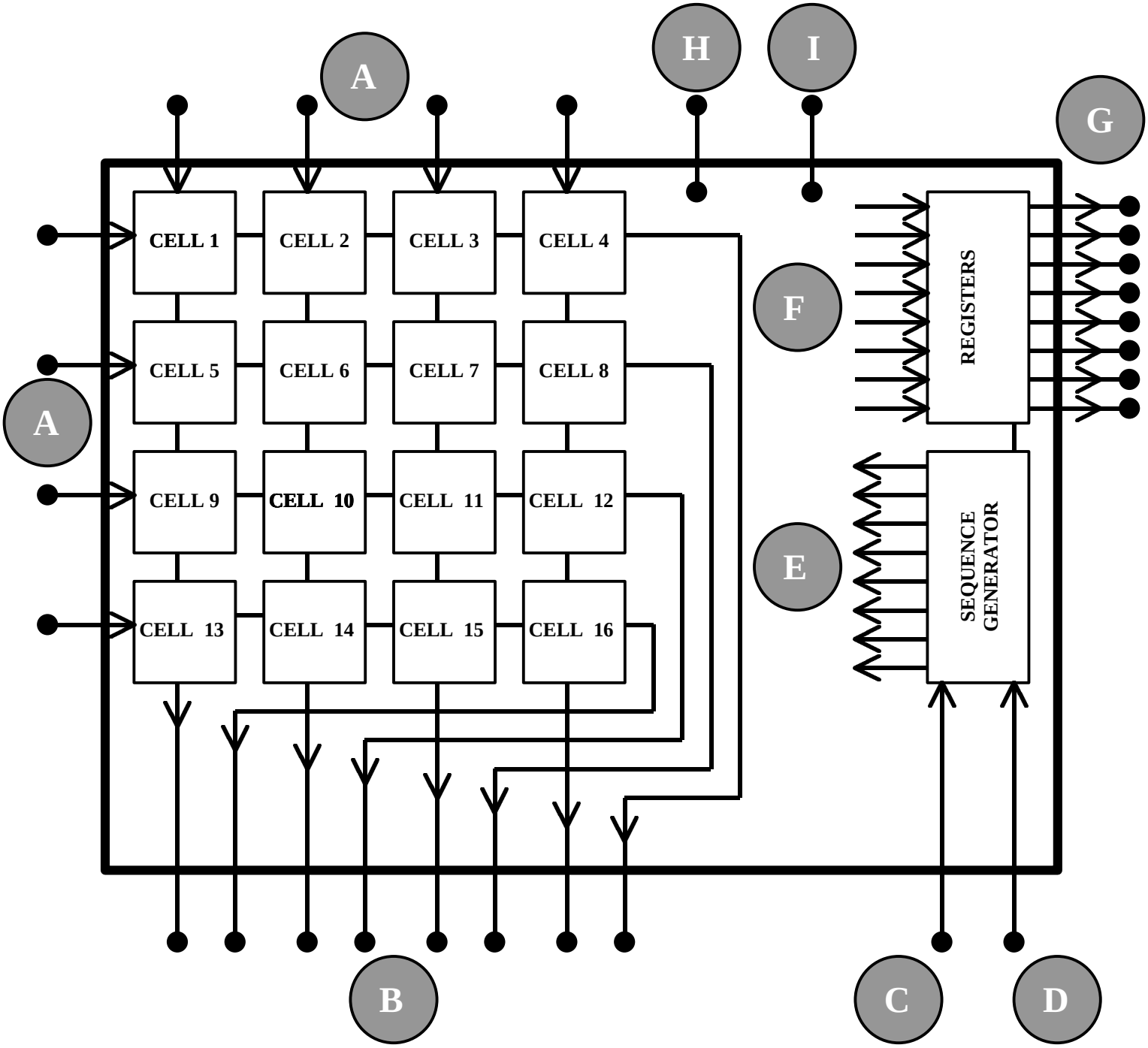
BLOCK DIAGRAM



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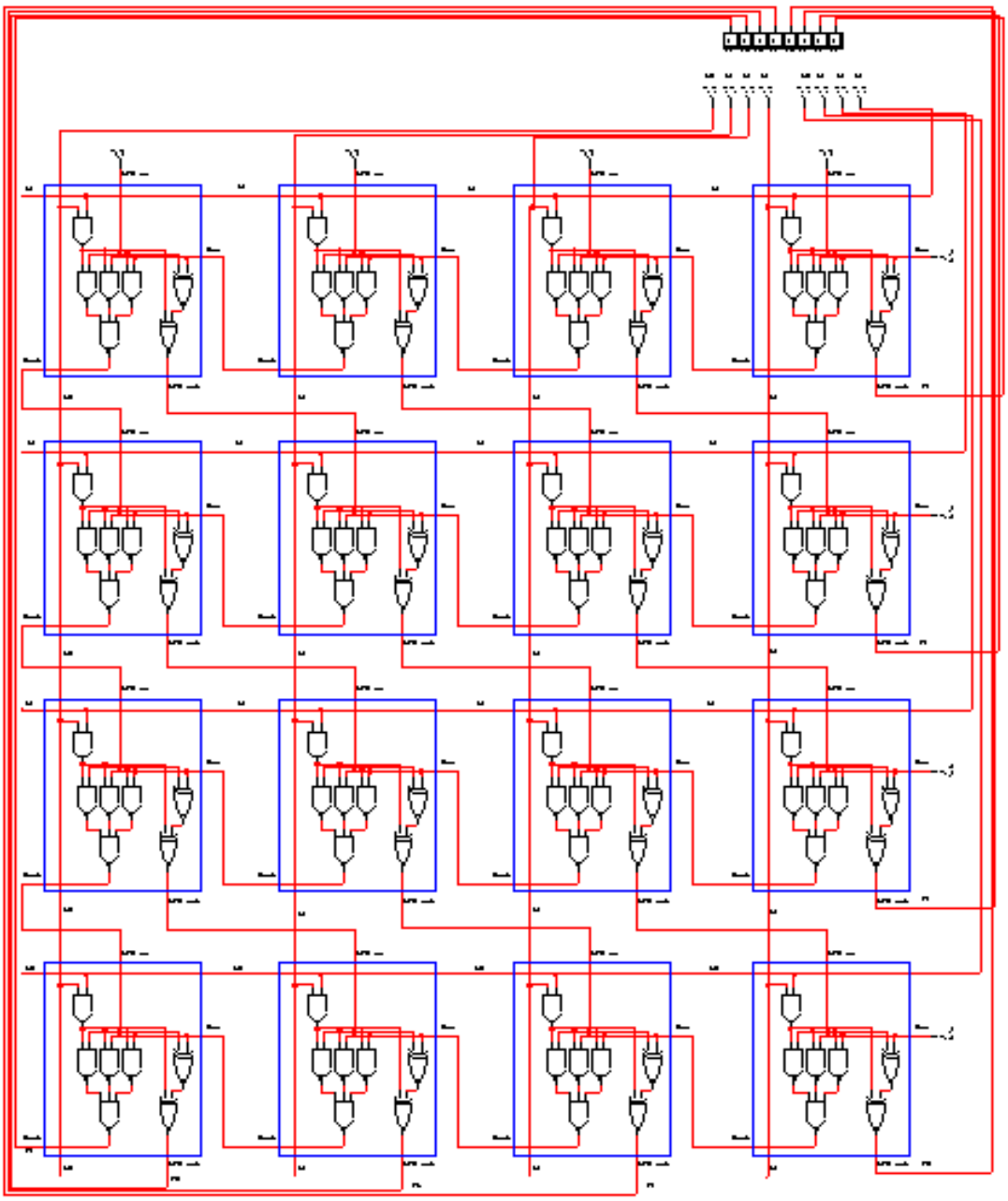
LOGIC WORKS SIMULATION



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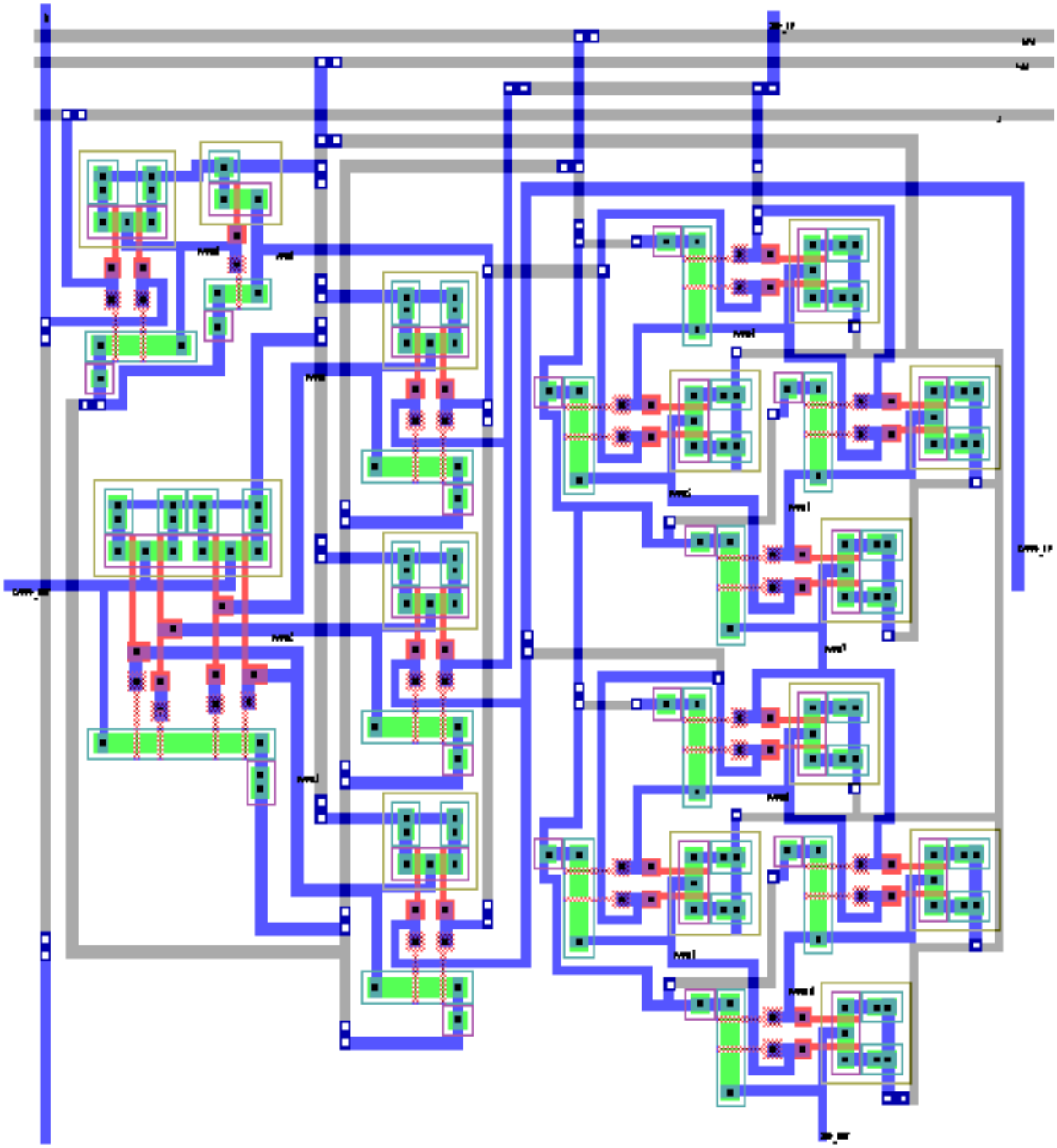
CMOS DESIGN USING L-EDIT



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PSPICE SIMULATION