PATENTS, STANDARDS, BIBLIOGRAPHY

PATENT SEARCH:

Internet Search – Applicable Patents

http://www.patents.ibm.com

KEYWORD – self testable (184 hits)

- Patent #US5173906: Built-in test for integrated circuits
- Patent #US5301199: Built-in self test circuit

KEYWORD – built-in testing (89 hits)

- Patent #US5790562: Circuit with built-in test and method thereof

KEYWORD – testable cellular array

- NO MATCHES FOUND

#US5173906: Built-in test for integrated circuits

Inventor(s): Dreibelbis; Jeffrey H. , Williston, VT 05495
Hedberg; Erik L. , Essex Junction, VT 05452
Petrovick, Jr.; John G. , Colchester, VT 05446

Abstract:

A built-in, i.e., on-chip, self-test system for a VLSI logic or memory module. A deterministic data pattern generator is provided on the VLSI chip, and operates to test a chip module and provide a fail/no-fail result, along with data identifying where the fail occurred. This location data is captured and made available for subsequent utilization. The built-in test circuitry is programmable, and is provided with a looping capability to provide enhanced burn-in testing, for example.

We claim:

1. A built-in (on-chip) self-tester for a VLSI circuit comprising:

- a data pattern generator, for generating predetermined deterministic data patterns for application to the data inputs of said circuit, wherein the data patterns are determined by way of codes applied to the self-tester.
- an address counter for generating addresses for application to the address inputs of said circuit in coordination with the generation of said data patterns;
- means for activating said data pattern generator and said address counter;
- means for comparing the results with expected data results and providing a pass/fail signal.

#US5301199: Built-in self test circuit

Inventor(s): Ikenaga; Takeshi , Kanagawa, Japan
Takahashi; Jun-ichi , Kanagawa, Japan

Abstract:

A built-in self test circuit includes a pattern generator, a functional block subjected to a self test on the basis of an output from the pattern generator, a space compressor for compressing a test result of the functional block, and a comparator for comparing an output from the space compressor with an expected value and outputting a comparison result. The functional block has O (positive integer) inputs and M (positive integer) outputs. The pattern generator is constituted by a linear feedback shift register, having an output bit width P (P=O/N) which is 1/N of the inputs O of the functional block, for generating a pseudorandom pattern and an iterative pseudorandom pattern output unit for distributing outputs from the linear feedback shift register in units of N outputs and outputting, to the functional block, an iterative pseudorandom pattern output having an iterative O-bit width (O=P*N) of the pseudorandom pattern output from the linear feedback shift register every P bits. The space compressor has a function of spatially compressing the M outputs from the functional block into L outputs (positive integer and M>L). The pattern generator, the functional block, the space compressor, and the comparator are built into a semiconductor chip into which other functional elements are built.

What is claimed is:

1. A built-in self test circuit comprising:

- a pattern generator;
- a functional block subjected to a self test on the bases of an output from said pattern generator;
- a space compressor for compressing a test result of said functional block; and
- a comparator for comparing an output from said space compressor with an expected value and outputting a comparison result,
- wherein said functional block includes a plurality of modules having the same function and has a data input bit width O (positive integer) and a data output bit width M (positive integer),
- said pattern generator is constituted by a linear feedback shift register, having an output bit width P which is an integer satisfied by the equation O/N<=P
- said space compressor has a function of spatially compressing the M outputs from said functional block into L outputs (positive integer and M>L), and

- said pattern generator, said functional block, said space compressor, and said comparator are built into a semiconductor chip into which other functional elements are built.

#US5790562: Circuit with built-in test and method thereof
Inventor(s): Murray; Brian Thomas , Novi, MI
Chakrabarty; Krishnendu , Norwood, MA
Hayes; John Patrick , Ann Arbor, MI

Abstract:

A circuit with a built-in self test, comprising: a circuit to be tested; a generating circuit coupled to the circuit to be tested, wherein the generating circuit generates (i) a series of input signals to the circuit to be tested and (ii) a series of reference signals; a space compaction circuit coupled to an output of the circuit to be tested, wherein the space compaction circuit uses a categorized response of the circuit to be tested to compact the output of the circuit to be tested by a maximum ratio and produces a series of output signals when the input signals are applied to the circuit to be tested; an analysis circuit coupled to the space compaction circuit and the generating circuit, providing a signal indicative of error in the circuit to be tested when the output signals fail to correspond to the reference signals.

We claim:

1. A built-in self test circuit method comprising the steps of:

- determining a response set of a circuit to be tested;
- pruning the response set by removing all vertices of the response set that have a degree of one;
- synthesizing a minimum required logic response of the response set by categorizing the pruned response set into a plurality of at least two categories, wherein no two adjacent vertices of the pruned response are in the same category, and carrying the categorization to the remainder of the response set; and
- implementing a space compaction circuit according to the minimum required logic response, wherein the space compaction circuit is responsive to the circuit to be tested and outputs an error signal in response to a defect in the circuit to be tested.

STANDARDS SEARCH:

Internet Search

http://www.nssn.org

KEYWORD – CMOS

- NO APPLICABLE STANDARDS (most applied to fabrication)

KEYWORD – VLSI

- NO APPLICABLE STANDARDS (most applied to fabrication)

http://standards.ieee.org

KEYWORD – CMOS

- NO APPLICABLE STANDARDS

KEYWORD – VLSI

- NO APPLICABLE STANDARDS

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