FUNCTIONAL DESCRIPTION

The main objective is to design testability features that can potentially be included in any CMOS chip. A 4-bit x 4-bit multiplier will be the circuit used to test the designed testability features. The VLSI design of the 4-bit x 4-bit multiplier circuit will contain sixteen cells. The testing features consist of a sequence generator and 8-bit registers for a signature analysis. The multiplier will have a total of eight inputs and eight outputs. The sequence generator, controlled by a clock and a start bit, will be used for cellular testing. The outputs of the sequence generator will be given to the user. Therefore, the expected outputs of the multiplier will also be known to the user based upon the multiplier truth table. The 8-bit registers will be used to store the information provided from the test. Outputs will also come from the registers for easy observation of the test's results.

The following are descriptions of the corresponding labels for the **BLOCK DIAGRAM**:

A) 4 x 4 MULTIPLIER INPUTS

Eight pins will be reserved for the inputs to the 4-bit x 4-bit multiplier circuit. According to the **BLOCK DIAGRAM,** these pins will be used for external use, but they will also be used internally to test the function of the 4-bit x 4-bit multiplier.

B) 4 x 4 MULTIPLIER OUTPUTS

Eight pins will also be reserved for the outputs of the 4-bit x 4-bit multiplier circuit. These pins are used externally as well as internally.

C) SEQUENCE GENERATOR START BIT

When set, the chip will begin its own diagnostic functions which will consist of a series of 8-bit words, given to the user, sent from the sequence generator to the inputs of the 4-bit x 4-bit multiplier. The external inputs and the normal outputs will be disregarded.

D) SEQUENCE GENERATOR CLOCK

This pin is reserved for an external clock. This clock drives the sequence generator and the registers.

E) REGISTER OUTPUTS

The 8-bit registers are used to store the outputs from the 4-bit x 4-bit multiplier when the chip is in test mode. The user will know the inputs from the sequence generator to the multiplier, and therefore will also know the expected outputs that are stored in the registers.

F) VOLTAGE SUPPLY

G) GROUND

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TESTABLE VLSI CIRCUIT DESIGN FOR CELLULAR ARRAYS

BLOCK DIAGRAM