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TESTABLE VLSI CIRCUIT DESIGN FOR CELLULAR ARRAYS

TMJL451-44A 4-bit x 4-bit Mulitplier With Built-In Cell Tester

The TMJL451-44A is a 4-bit x 4-bit multiplier

The CMOS design of the 4-bit x 4-bit multiplier circuit contains sixteen cells. The testing features

for a signature analysis. The sequence generator, controlled by a clock and a start bit, is used for

generator are given in Table 1. The expected are

based upon a multiplier truth table. The 8-bit are used to store the information provided from the test. Outputs come from the registers for easy observation of the test's results.

Features

- □ Low cost / CMOS technology
- □ Fully functional 4-bit x 4-bit multiplier
- □ Testable cellular array
- □ Single-clock-driven sequence generator and registers
- □ Start/stop bit to begin, interrupt, and end diagnostic testing
- □ 8-bit register for easy viewing of test results

Connection Diagram

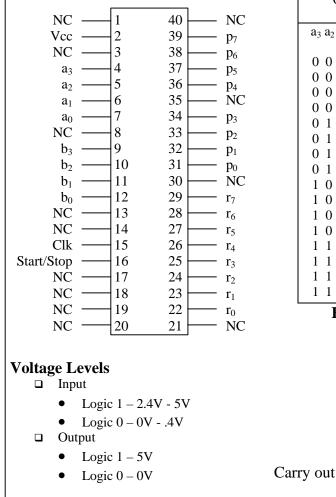


Table 1 – Sequence Generator	
Outputs From	Expected Outputs
Generator	From Multiplier
$a_3 a_2 a_1 a_0 b_3 b_2 b_1 b_0$	$p_7 \ p_6 \ p_5 \ p_4 \ p_3 \ p_2 \ p_1 \ p_0$
0000 0000	0 0 0 0 0 0 0 0 0
0 0 0 1 0 0 0 1	0000 0001
0010 0010	0 0 0 0 0 1 0 0
0011 0011	0 0 0 0 1 0 0 1
0100 0100	0 0 0 1 0 0 0 0
0101 0101	0 0 0 1 1 0 0 1
0110 0110	0010 0100
0111 0111	0011 0001
1000 1000	0100 0000
1001 1001	0 1 0 1 0 0 0 1
1010 1010	0110 0100
1011 1011	0 1 1 1 1 0 0 1
1 1 0 0 1 1 0 0	1001 0000
1 1 0 1 1 1 0 1	1010 1001
1 1 1 0 1 1 1 0	1 1 0 0 0 1 0 0
1111 1111	$1 \ 1 \ 1 \ 0 \ 0 \ 0 \ 1$
Figure 1 – Single Cell Schematic	
b _i Sum in	
	ai
∢ │	
	Carry in
	/

Σ

▼ Sum out

Table 1 – Sequence Generator