Jarrod Luker Tim McKinney

TESTABLE VLSI CIRCUIT DESIGN FOR CELLULAR ARRAYS

To: Dr. Brian Huggins

CC: Dr. V. Prasad

From: Jarrod Luker

Tim McKinney

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Re: Project Confirmation

Under the supervision of Dr. V. Prasad, Tim McKinney and Jarrod Luker will be doing **TESTABLE VLSI CIRCUIT DESIGN FOR CELLULAR ARRAYS** for our senior project.

The main objective is to design testability features that can potentially be included in any CMOS chip. A 4-bit x 4-bit multiplier will be the circuit used to test the designed testability features. The VLSI design of the 4-bit x 4-bit multiplier circuit will contain sixteen cells. The testing features consist of a sequence generator and 8-bit registers for a signature analysis. The multiplier will have a total of eight inputs and eight outputs. The sequence generator, controlled by a clock and a start bit, will be used for cellular testing. The outputs of the sequence generator will be given to the user. Therefore, the expected outputs of the multiplier will also be known to the user based upon the multiplier truth table. The 8-bit registers will be used to store the information provided from the test. Outputs will also come from the registers for easy observation of the test's results.