Summary:

For this senior project, an integrated circuit that will multiply a three bit vector with a three bit by three bit matrix will be designed. This chip will take the user-supplied inputs for each matrix element, the vector elements, and control signals, and output a six bit vector. This circuit will be designed on the VLSI level, using L-Edit™ to design and connect each gate and component of the chip. Once this circuit is designed, it will be sent to a manufacturer to have the chip fabricated, using funding from a NSF grant.

Functional Description of Project:

The Matrix-Vector Multiplier Chip is designed to provide synchronous multiplication of a three bit vector by a three bit by three bit matrix at a relatively high speed. A sequence generator will be included if there is enough space left after the rest of the circuit has been designed. There is a set die size allotted to our project that the total area of the circuit may not exceed. This sequence generator will provide test inputs for both the vector and matrix elements, and test the outputs to make sure the circuit is functioning properly. There will be a specific input called Mode that will switch the circuit from normal operation to test mode (using the sequence generator). A list of inputs to and outputs from the system[10] is shown below in tabular form. Since we are still designing the circuit, some parts of the project will be unknown until the project is actually completed (see control signals below).

Inputs to System	Description
A1	1st element of 1st row of matrix
A2	2nd element of 1st row of matrix
A3	3rd element of 1st row of matrix
B1	1st element of 2nd row of matrix
B2	2nd element of 2nd row of matrix
B3	3rd element of 3rd row of matrix
C1	1st element of 3rd row of matrix
C2	2nd element of 3rd row of matrix
C3	3rd element of 3rd row of matrix
X1	1st element of input vector
X2	2nd element of input vector
X3	3rd element of input vector
Vcc	Provides power to circuit
Ground	Provides discharging path to circuit
Mode	Selects either normal or test mode
Clock	Provides timing signal to circuit
Control Signals	As yet unspecified control signals

Outputs from System	Description
Y1	1st term of output vector (2 bits in length)[11]
Y2	2nd term of output vector (2 bits in length)
Y3	3rd term of output vector (2 bits in length)
Test	Shows if circuit failed the test mode or not

These two tables above show the inputs and outputs from the system when the whole system is viewed as on big block. Another way of looking at, these inputs and outputs are what the user will "see" and deal with when connecting the chip to their circuit. The user will need to supply all the inputs mentioned above. Once the inputs have been supplied, the outputs shown above will be observed on certain pins of the chip. To gain a more in-depth view of our circuit, the System-Level Block Diagram has been included. The block diagram shows the circuit as several major "blocks," each of which has a specific function. Each of the blocks' functions will be explained in detail.