

EE 311 – Digital Hardware Organization - 3 hours
Required Course (substitute for EE 201, 201 for transfer students)

1. *2007-2008 Catalog description*

Introduction to logic design with focus on the following topics: fundamentals of Boolean algebra and minimization techniques, logic realizations of SOP and POS functions, multiple function synthesis using PLDs, combinational circuit design as it applies to computers, sequential circuit elements, flip flops, counters and shift-registers, clock generation circuits, algorithmic state machine method of designing sequential circuits, and VHDL design and synthesis. Not open to students with credit in EE 101 or EE 201.

2. *Prerequisites by topic*

None

3. *Textbook (s) and/or other required material*

Required Text: Digital Design – Principles and Practices, 4th ed., by Wakerly, Pearson/Prentice Hall

Recommended Texts: The VHDL Reference, by Heinkel et. al., Wiley

The Designer's Guide to VHDL, 2nd ed., by Ashenden, Morgan Kaufmann

Class Software: Quartus II, ver. 5 or later, www.altera.com/products/software/products/quartus2/qts-index.html

by Altera, <http://www.altera.com/>

All course material is posted on Blackboard allowing online student access.

4. *Class/Laboratory Schedule*

Three sessions per week, each 50 minutes, for 14 weeks plus 2 hour final time slot

5. *Topics Covered (Outcomes influenced)*

- Boolean algebra, Huntington's Postulates, proof of theorems via Boolean algebra and truth tables, DeMorgan's laws (7ab)
- Number representation, binary, hex, one's and two's complement, binary arithmetic (7a)
- Hardware gates and logic functions: AND, OR, NOT, XOR, NAND, NOR (7cd)
- Analysis and design of combinational logic networks: truth tables, circuit minimization via Boolean algebra and Karnaugh maps, hazards, NAND/NOR synthesis (7bcd)
- Arithmetic circuits: half & full adders; parallel, serial, and carry look ahead adders; multipliers (7bcd)
- Design with complex digital components: multiplexers, decoders, encoders, PAL's, CPLD's, and FPGA's. (7abcdef)
- Introduction to VHDL synthesis of combinational logic circuits via structural, dataflow, and behavioral modeling. (7fg)
- Sequential circuit components: SR, D, JK, and T flip flops. (7efgh)
- Sequential circuit design: state diagrams, present/next state tables, and algorithmic state machine (ASM) flowcharts. (7efgh)
- MSI sequential circuit components: shift registers and counters. (7ef)
- Introduction to VHDL synthesis of sequential logic circuits via behavioral modeling. (7efgh)

6. *Contribution of course to meeting the curriculum components*

Engineering Science - 50%, Engineering Design - 50%

7. *Course Outcomes (Program Outcome contributions): In learning the course topics, the student will attain the following outcomes*

- a) Student will use the binary and hexadecimal representations of physical data, numbers, alphanumeric characters, binary codes, binary arithmetic, complement representation. (9A,B)
- b) Student will use basic postulates of Boolean algebra and binary operators in theorem proofs (9A)
- c) Student will learn the logic vs. hardware description of Boolean operators – AND, OR, NOT, XOR, NAND, NOR (9B)
- d) Student will perform traditional combinational logic analysis and design including minimization (9A,B,D)
- e) Student will perform traditional synchronous sequential circuit analysis and design. (9A, B, C, D)
- f) Student will learn the basic design of complex logic devices and use them in digital logic design (9A, B, C, D)
- g) Student will learn the fundamental concepts of a hardware description language

- h) Student will use a professional level computer-aided design (CAD) package for design, simulation, and synthesis. (9B, C, D)
- i) Student will design, simulate, synthesize in hardware, and demonstrate a combinational logic project using the hardware description language and CAD package referenced above. (9A, B, C, D, G)
- j) Student will design, simulate, synthesize in hardware, and demonstrate a finite state machine project using the hardware description language and CAD package referenced above. (9A, B, C, D, G)

8. *Grading policy and criteria:*

The course grade will be based upon the percentage of points earned throughout the semester. The points are earned based upon how well you meet the objectives stated above. Each objective will be tested several times and ways throughout the semester to assure accurate evaluation. The points assigned for your efforts will conform to the Undergraduate Catalog, Gradepoint System. The initial grade ranges, in percent, are: 100 – A – 85 – B – 72 – C – 58 – D – 45 – F – 0. [test(ea) = 100; peer review(tot) = 300; project 1 = 100, project 2 = 200

A grade of C corresponds to meeting the minimum competency required to understand course topics and attain course outcomes.”

9. *Relationship of course to program outcomes*

label	Program Outcomes (A Graduate from the program will:)	Contribution
A	have knowledge of the mathematical and scientific foundation of electrical engineering	Strong
B	have knowledge of and the ability to apply techniques and technology of electrical engineering	Strong
C	complete a design project sequence, culminating in a capstone project at or near the professional level	Moderate
D	understand that acquisition of new knowledge is needed for success in the electrical engineering profession	Moderate
E	meet Bradley’s general education requirements which are based on the principles of liberal education	NA
F	have experience in communicating technical information and working on teams	Foundational
G	understand the importance of professional and ethical behavior	Moderate

10. *Prepared by:* James Irwin – 08 06 02