

EE 101 - Introductory Electrical Engineering - 1 Hour
Required course

1. *2007-2008 Course Catalog description*

Introductory course focusing on logic design on the following topics: fundamentals of Boolean algebra and minimization techniques, combinational logic realization of SOP and POS functions, and multiple function synthesis using PLDs. In addition, students view various presentations of significant historical electrical engineers and topics.

2. *Prerequisites by topics*

None

3. *Textbook and/or other required materials*

Required textbook: Electric Fundamentals of Digital Logic, Stephen Brown and Zvonko Vranesic, McGraw Hill Publishing, Second Edition, 2005.

Required Software: Quartus II (ver. 5 or later) by Altera (<http://www.altera.com/>)
(Free download at: www.altera.com/products/software/products/quartus2/qts-index.html)

4. *Class Schedule*

Seventeen lecture class sessions per semester (each 50 minutes in length), two hourly exams, a final exam, and a design project.

5. *Topics Covered (outcomes influenced)*

- Proof of theorems and simplification of Boolean expressions via Boolean algebra. (7a, b, c)
- Number representations and arithmetic: binary, hex, one's and two's complement. (7a)
- Hardware gates and logic functions: AND, OR, NOT, NAND, NOR, XOR, and XNOR (7a, c, d, e, f)
- Analysis and design of combinational logic networks: truth tables, circuit minimization via Boolean algebra and Karnaugh maps, sum of products, products of sums, and NAND/NOR synthesis (7a, c, d, e, f)
- Arithmetic circuits: half and full adders (7a, c, d, e)
- Combinational logic design with small scale integrated circuits (7a, c, d, e)
- Combinational logic circuit design and simulation using the Altera Quartus II block diagram editor and simulator. (7a, d, e)
- Combinational logic design project: designed, simulated, implemented, and laboratory tested on a CPLD via the Altera Quartus II Integrated Development Environment (IDE). (7a, c, d, e, f)
- ECE Student Code of Conduct (7g)

6. *Contribution of the course to meeting the professional component*

Engineering science - 50%, Engineering design - 50%

7. *Course Outcomes (Program Outcome contributions)*

- a) Students will use the binary and hexadecimal representations of numbers, binary arithmetic, and complement representations. (9A, B)
- b) Students will use binary operators and basic Boolean algebra postulates to prove Boolean theorems. (9A)
- c) Students will use binary operators and Boolean algebra theorems to minimize Boolean expressions. (9A, B)
- d) Students will use the hardware description of Boolean operators (AND, OR, NOT, NAND, NOR, XOR, XNOR). (9B, D)
- e) Students will use combinational logic design, including minimization of circuits via Boolean algebra and Karnaugh maps. (9A, B, D)
- f) Students will use the schematic capture capabilities of an Integrated Development Environment (IDE) package for digital logic design and simulation, culminating in the design and implementation of a group project. (9B, C, D, F, G)
- g) Student will understand the ECE Student Code of Conduct (9G)

8. *Grading Policy*

The level to which the students achieve the course objectives is determined by the following grading policy.

Grades will be dictated by the results of two one-hour exams, a comprehensive final exam, and a team design project based on the following percentages.

- Exam 1: 75 points (21.5%)
- Exam 2: 75 points (21.5%)
- Final Exam: 150 points (42.8%)
- Team Project: 50 points (14.2%)

Each student's portion of the group design project is to be completed independently by each student. Therefore, students are expected to design their portion of the group project with assistance obtained exclusively from the instructor, and collaboration between students will be considered a form of cheating. Letter grades will be assigned for each exam to provide students with a grade estimate throughout the semester, but the final course grade will be determined by a curve based on the combined numerical results of all three exams and the group design project. Although the arithmetic mean of the combined numerical results will usually correspond to a "middle" B, the letter grade corresponding to the arithmetic mean may be shifted up or down based on the performance of the present class with respect to the degree to which students meet the course outcomes specified in item 7 above. A grade of 'C' corresponds to minimum acceptable level of competency relative to the course outcomes. Exams missed without prior approval will result in a zero for that exam. In addition, cheating on examinations or projects will be dealt with as described in the Bradley University Academic Handbook.

9. *Relationship of course to program outcomes*

label	Program Outcomes (A Graduate from the program will:)	Contribution
A	have knowledge of the mathematical and scientific foundation of electrical engineering	Strong
B	have knowledge of and the ability to apply techniques and technology of electrical engineering	Strong
C	complete a design project sequence, culminating in a capstone project at or near the professional level	Foundational
D	understand that acquisition of new knowledge is needed for success in the electrical engineering profession	Moderate
E	meet Bradley's general education requirements which are based on the principles of liberal education	NA
F	have experience in communicating technical information and working on teams	Moderate
G	understand the importance of professional and ethical behavior	Strong

10. *Prepared by:* S. D. Gutschlag:

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